FORM PTO-1390 (REV. 12-2001) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY 'S DOCKET NUMBER: 32226.17

U S APPLICATION NO. (If known, see 37 CFR 1.5): N/A 10/070025

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/01607	18 May 2000	25 August 1999

TITLE OF INVENTION: **Elektronische Schaltung mit ferroelektrischen Flipflops**

APPLICANT(S) FOR DO/EO/US: **Infineon Technologies AG**

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [X] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [ ] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [X] is attached hereto (required only if not communicated by the International Bureau).
   b. [ ] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [X] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [ ] Amendments to the claims of the International Aplication under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [ ] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [ ] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16. [ ] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [ ] Other items or information:

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Mary A. Flores

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(Signature of person mailing paper or fee)

U.S. APPLICATION NO (If known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
NA/ 10/070025	PCT/DE00/01607	32226.17

21. [X] The following fees are submitted:	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890	
Surcharge of **$130.00** for furnishing the oath or declaration later than [X] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 130	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	$
Total claims	26 - 20 =	6	x **$18.00**	$ 108
Independent claims	1 - 3 =	0	x **$84.00**	$ 0
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$280.00**	$ 0

TOTAL OF ABOVE CALCULATIONS =	$ 1,128	
[ ] Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2. +	$	
SUBTOTAL =	$ 1,128	
Processing fee of **$130.00** for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)).	$ 0	
TOTAL NATIONAL FEE =	$ 1,128	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +	$ 0	
TOTAL FEES ENCLOSED =	$ 1,128	
	Amount to be refunded:	$
	charged:	$

a. [X] A check in the amount of $ 1,128 to cover the above fees is enclosed.

b. [ ] Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 02-3732 . A duplicate copy of this sheet is enclosed.

d. [ ] Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

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SIGNATURE

JEFFREY R. STONE

NAME

47,976

REGISTRATION NUMBER

#4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re:	U.S. Patent Application 10/070025	PATENT
German Title:	Elektronische Schaltung mit Ferroelektrischen Flipflops	
English Translation:	Electronic Circuit for a Method for Storing Information with Ferroelectric Flip-Flops	
Applicant:	Infineon Technologies, AG	
Inventors:	Christl Lauterbach Georg Braun Udo Ollert Werner Weber	
Attorney Docket No:	32226.17	

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

PRELIMINARY AMENDMENT

In the above-entitled patent application, please amend the application as follows:

In the Claims

1. (amended) 1. Electronic circuit, comprising an input for inputting at least one information signal; an energy means for converting energy contained in the at least one information signal into a voltage supply; a control means for generating at least one switch-on control signal when an information signal arrives; and a signal processing means for storing an information item represented by the at least one information signal by means of at least one ferroelectric flip-flop and/or for evaluating an information item represented by the at least one information signal and storing the secondary information obtained through the evaluation by means of the at least one ferroelectric flip-flop; wherein the signal processing means can be

activated by the at least one switch-on control signal for the purpose of evaluation and/or storage; and wherein, during the evaluation and/or storage, the at least one information signal may be or is the sole energy source for the electronic circuit.

2. (amended) The electronic circuit as claimed in claim 1, wherein the control means can generate at least one switch-off control signal after a predetermined time has elapsed after the at least one information signal arrives or when the energy converted from the at least one information signal is exhausted, wherein the signal processing means can be caused or is caused to effect a storage and to effect deactivation by the at least one switch-off control signal.

3. (amended) The electronic circuit as claimed in claim 1, wherein the information stored in the at least one ferroelectric flip-flop can be converted into at least one output signal by the signal processing means and the electronic circuit furthermore has at least one output for outputting the at least one output signal.

4. (amended) The electronic circuit as claimed in claim 1, wherein the electronic circuit furthermore has a display means for displaying the information stored in the at least one ferroelectric flip-flop.

5. (amended) The electronic circuit as claimed in claim 4, wherein the display means is concomitantly supplied by the voltage supply generated by the energy means.

6. (amended) The electronic circuit as claimed in claim 4, wherein the display means has an LCD display.

7. (amended) The electronic circuit as claimed in claim 3, wherein an external voltage supply and external control means can be connected for the outputting of the information stored in the at least one ferroelectric flip-flop by the signal processing means.

8. (amended) The electronic circuit as claimed in claim 1, wherein the at least one switch-on control signal is comprised of the following signals: an activation signal (PRECH) for activating precharge transistors of the at least one ferroelectric flip-flop; a transfer signal (PLN) for transferring the information contained in ferroelectric capacitors of the at least one ferroelectric flip-flop onto internal data lines of the at least one ferroelectric flip-flop; and a current switching signal (NSET) for switching on the voltage supply of the signal processing means.

9. (amended) The electronic circuit as claimed in claim 2, wherein the at least one switch-off control signal is comprised of the following signals: a transfer end signal (PLN); an activation signal (PRECH) for activating precharge transistors of the at least one ferroelectric flip-flop; and a current switch-off signal (NSET) for switching off the voltage supply of the signal processing means.

10. (amended) The electronic circuit as claimed in claim 8, wherein signal lines for each of the switch-on signals lead from the control means to the signal processing means.

11. (amended) The electronic circuit as claimed in claim 9, wherein signal lines for each of the switch-off signals lead from the control means to the signal processing means.

12. (amended) The electronic circuit as claimed in claim 11, characterized in that, for the transfer signal and the transfer end signal, a common transfer signal line leads from the control means to the signal processing means, the transfer signal consists in the application of a voltage to the common transfer signal line and the transfer end signal consists in the disconnection of the voltage on the common transfer signal line.

13. (amended) The electronic circuit as claimed in claim 11, characterized in that, for the current switching signal and the current switch-off signal, a common current signal line leads from the control means to the signal processing means, the current switching signal consists in the application of a voltage to the common current signal line and the current switch-off signal consists in the disconnection of the voltage on the common current signal line.

14. (amended) The electronic circuit as claimed in claim 1, wherein the signal processing circuit is a counting circuit for evaluating a plurality of information signals, which arrive successively or simultaneously, by counting the information signals that have arrived.

15. (amended) The electronic circuit as claimed in claim 14, wherein the counting circuit comprises a plurality of cascaded edge-controlled ferroelectric flip-flops, in which the at least one information signal is input into the clock input (CLK) of the first ferroelectric flip-flop of the plurality of cascaded ferroelectric flip-flops and the output (Q) of each of the ferroelectric flip-flops, except for the last, is in each case also connected to the clock input (CLK) of the ferroelectric flip-flop connected downstream.

16. (amended) A method for storing information comprising at least one information signal or information obtained through evaluation of the at least one information signal in at least one ferroelectric flip-flop in a signal processing means, having the following steps: A: generating at least one switch-on control signal from an information signal that has arrived, and generating a voltage supply from energy contained in the at least one information signal; B: activating the signal processing means by the switch-on control signal and applying the voltage supply to the signal processing means; C: storing an information item represented by the at least one information signal by means of at least one ferroelectric flip-flop and/or evaluating an information item represented by the at least one information signal and storing the secondary information obtained through the evaluation by means of at least one ferroelectric flip-flop; D: generating a switch-off control signal after a predetermined time has elapsed after the at least one information signal arrives and/or when the energy converted from the at least one information signal is exhausted; and E: deactivating the signal processing means by the switch-off control signal.

17. (amended) The method as claimed in claim 16, wherein step B further comprises the sub-steps: B1: activating precharge transistors of the at least one ferroelectric flip-flop by applying a voltage: B2: deactivating the precharge transistors of the at least one ferroelectric flip-flop by disconnecting the voltage; B3: applying a voltage to ferroelectric capacitors of the at least one ferroelectric flip-flop for transferring the information stored in the ferroelectric capacitors to logic gates of the at least one ferroelectric flip-flop; and B4: activating the voltage supply of the logic gates of the at least one ferroelectric flip-flop.

18. (amended) The method as claimed in claim 16, wherein step E further comprises the sub-steps: E1: disconnecting a voltage present across ferroelectric capacitors of the at least

one ferroelectric flip-flop; E2: deactivating the voltage supply of the logic gates of the at least one ferroelectric flip-flop; E3: activating precharge transistors of the at least one ferroelectric flip-flop by applying a voltage; and E4: deactivating the precharge transistors of the at least one ferroelectric flip-flop by disconnecting the voltage.

19. (amended) The method as claimed in claim 16, wherein the electronic circuit contains a plurality of ferroelectric flip-flops and the evaluation comprises a summation of the value represented by the information signal and a value already stored in the ferroelectric flip-flops.

20. (amended) The method as claimed in claim 19, wherein the summation is effected by means of a counting operation in which the plurality of ferroelectric flip-flops are cascaded in a counter arrangement and an arriving information signal increments or decrements a counter reading of the counter arrangement by the value 1.

21. (amended) The method as claimed in claim 16, wherein the information stored in the at least one ferroelectric flip-flop can be converted into at least one output signal and be output from the electronic circuit.

22. (amended) The use of ferroelectric flip-flops for electronic circuits, wherein the electronic circuit can detect and/or evaluate information signals and results of the detection and/or evaluation can be stored in at least one ferroelectric flip-flop, characterized in that the entire energy required for the detection, processing and storage can be generated from the information signal.

23. (amended) The use as claimed in claim 22, wherein the evaluation comprises counting the arriving information signals.

24. (amended) The use as claimed in claim 23, wherein the electronic circuit can count up or count down arriving information signals.

25. (amended) The use as claimed in claim 22, wherein the electronic circuit is used in a liquid counter.

26. (amended) A liquid counter for determining the flow of liquids through a system, comprising: a sensor which can generate or generates information signals depending on a quantity of liquid flowing through the system; and an electronic circuit as claimed in claim 1 for counting the information signals generated by the sensor; wherein the information signals are the sole energy source for the electronic circuit.

In the Claims

1. (amended) 1. Electronic circuit [(1)], [having] comprising an input [(5)] for inputting at least one information signal; an energy means [(2)] for converting energy contained in the at least one information signal into a voltage supply; a control means [(3)] for generating at least one switch-on control signal when an information signal arrives; and a signal processing means [(4)] for storing an information item represented by the at least one information signal by means of at least one ferroelectric flip-flop and/or for evaluating an information item represented by the at least one information signal and storing the secondary information obtained through the evaluation by means of the at least one ferroelectric flip-flop [(26)]; wherein the signal processing means [(4)] can be activated by the at least one switch-on control signal for the purpose of evaluation and/or storage; and wherein, during the evaluation and/or storage, the at least one information signal may be or is the sole energy source for the electronic circuit [(1)].

2. (amended) The electronic circuit as claimed in claim 1, [characterized in that] wherein the control means [(3)] can generate at least one switch-off control signal after a predetermined time has elapsed after the at least one information signal arrives [and/]or when the energy converted from the at least one information signal is exhausted, wherein the signal processing means [(4)] can be caused or is caused to effect a storage and to effect deactivation by the at least one switch-off control signal.

3. (amended) The electronic circuit [(1)] as claimed in claim 1 [or 2], [characterized in that] wherein the information stored in the at least one ferroelectric flip-flop [(26)] can be converted into at least one output signal by the signal processing means [(4)] and the electronic circuit [(1)] furthermore has at least one output [(6)] for outputting the at least one output signal.

4. (amended) The electronic circuit[s] [(1)] as claimed in [one of] claim[s] 1 [to 3], [characterized in that] wherein the electronic circuit furthermore has a display means [(10)] for displaying the information stored in the at least one ferroelectric flip-flop [(26)].

5. (amended) The electronic circuit [(1)] as claimed in claim 4, [characterized in that] wherein the display means [(10)] is concomitantly supplied by the voltage supply generated by the energy means [(2)].

6. (amended) The electronic circuit [(1)] as claimed in claim 4 [or 5], [characterized in that] wherein the display means [(10)] has an LCD display [(11)].

7. (amended) The electronic circuit [(1)] as claimed in [one of] claim[s] 3 [to 6], [characterized in that] wherein an external voltage supply and external control means can be connected for the outputting of the information stored in the at least one ferroelectric flip-flop [(26)] by the signal processing means [(4)].

8. (amended) The electronic circuit [(1)] as claimed in [one of] claim[s] 1 [to 7], [characterized in that] wherein the at least one switch-on control signal [has] is comprised of the following signals: an activation signal (PRECH) for activating precharge transistors [(18,19)] of the at least one ferroelectric flip-flop [(26)]; a transfer signal (PLN) for transferring the information contained in ferroelectric capacitors [(14,15)] of the at least one ferroelectric flip-flop [(26)] onto internal data lines [(22,23)] of the at least one ferroelectric flip-flop [(26)]; and a current switching signal (NSET) for switching on the voltage supply of the signal processing means [(4)].

9. (amended) The electronic circuit [(1)] as claimed in [one of] claim[s] 2 [to 8], [characterized in that] wherein the at least one switch-off control signal [has] is comprised of the following signals: a transfer end signal (PLN); an activation signal (PRECH) for activating precharge transistors [(18,19)] of the at least one ferroelectric flip-flop [(26)]; and a current switch-off signal (NSET) for switching off the voltage supply of the signal processing means [(4)].

10. (amended) The electronic circuit [(1)] as claimed in claim 8 [or 9], [characterized in that] wherein signal lines [(8)] for each of the switch-on signals lead from the control means [(3)] to the signal processing means [(4)].

11. (amended) The electronic circuit [(1)] as claimed in claim 9 [or 10], [characterized in that] wherein signal lines [(8)] for each of the switch-off signals lead from the control means [(3)] to the signal processing means [(4)].

12. (amended) The electronic circuit [(1)] as claimed in claim 11, characterized in that, for the transfer signal and the transfer end signal, a common transfer signal line leads from the control means [(3)] to the signal processing means [(4)], the transfer signal consists in the application of a voltage to the common transfer signal line and the transfer end signal consists in the disconnection of the voltage on the common transfer signal line.

13. (amended) The electronic circuit [(1)] as claimed in claim 11 [or 12], characterized in that, for the current switching signal and the current switch-off signal, a common current signal line leads from the control means [(3)] to the signal processing means [(4)], the current switching signal consists in the application of a voltage to the common current signal line and the current switch-off signal consists in the disconnection of the voltage on the common current signal line.

14. (amended) The electronic circuit [(1)] as claimed in [one of] claim[s] 1 [to 13], [characterized in that] <u>wherein</u> the signal processing circuit [(4)] is a counting circuit for evaluating a plurality of information signals, which arrive successively or simultaneously, by counting the information signals that have arrived.

15. (amended) The electronic circuit [(1)] as claimed in claim 14, [characterized in that] <u>wherein</u> the counting circuit comprises a plurality of cascaded edge-controlled ferroelectric flip-flops [(34)], in which the at least one information signal is input into the clock input (CLK) of the first ferroelectric flip-flop [(34)] of the plurality of cascaded ferroelectric flip-flops [(34)] and the output (Q) of each of the ferroelectric flip-flops [(34)], except for the last, is in each case also connected to the clock input (CLK) of the ferroelectric flip-flop [(34)] connected downstream.

16. (amended) A method for storing information [represented by] comprising at least one information signal or information obtained through evaluation of the at least one information signal in at least one ferroelectric flip-flop [(26)] in a signal processing means [(4)], having the following steps: A: generating at least one switch-on control signal from an information signal that has arrived, and generating a voltage supply from energy contained in the at least one information signal; B: activating the signal processing means [(4)] by the switch-on control signal and applying the voltage supply to the signal processing means [(4)]; C: storing an information item represented by the at least one information signal by means of at least one ferroelectric flip-flop and/or evaluating an information item represented by the at least one information signal and storing the secondary information obtained through the evaluation by means of at least one ferroelectric flip-flop [(26)]; D: generating a switch-off control signal after a predetermined time has elapsed after the at least one information signal arrives and/or when the energy converted from the at least one information signal is exhausted; and E: deactivating the signal processing means [(4)] by the switch-off control signal.

17. (amended) The method as claimed in claim 16, [characterized in that] wherein step B [has] further comprises the sub-steps: B1: activating precharge transistors [(18,19)] of the at least one ferroelectric flip-flop [(26)] by applying a voltage: B2: deactivating the precharge transistors [(18,19)] of the at least one ferroelectric flip-flop [(26)] by disconnecting the voltage; B3: applying a voltage to ferroelectric capacitors [(14,15)] of the at least one ferroelectric flip-flop [(26)] for transferring the information stored in the ferroelectric capacitors [(14,15)] to logic gates [(12,13,24,25)] of the at least one ferroelectric flip-flop [(26)]; and B4: activating the voltage supply of the logic gates [(12,13,24,25)] of the at least one ferroelectric flip-flop [(26)].

18. (amended) The method as claimed in claim 16 [or 17], [characterized in that] wherein step E [has] further comprises the sub-steps: E1: disconnecting a voltage present across ferroelectric capacitors [(14,15)] of the at least one ferroelectric flip-flop [(26)]; E2: deactivating the voltage supply of the logic gates [(12,13,24,25)] of the at least one ferroelectric flip-flop [(26)]; E3: activating precharge transistors [(18,19)] of the at least one ferroelectric flip-flop [(26)] by applying a voltage; and E4: deactivating the precharge transistors [(18,19)] of the at least one ferroelectric flip-flop [(26)] by disconnecting the voltage.

19. (amended) The method as claimed in [one of] claim[s] 16 [to 18], [characterized in that] wherein the electronic circuit [(1)] contains a plurality of ferroelectric flip-flops [(26)] and the evaluation comprises a summation of the value represented by the information signal and a value already stored in the ferroelectric flip-flops [(26)].

20. (amended) The method as claimed in claim 19, [characterized in that] wherein the summation is effected by means of a counting operation in which the plurality of ferroelectric flip-flops [(26)] are cascaded in a counter arrangement and an arriving information signal increments or decrements a counter reading of the counter arrangement by the value 1.

21. (amended) The method as claimed in [one of] claim[s] 16 [to 20], [characterized in that] wherein the information stored in the at least one ferroelectric flip-flop [(26)] can be converted into at least one output signal and be output from the electronic circuit [(1)].

22. (amended) The use of ferroelectric flip-flops [(26)] for electronic circuits, wherein the electronic circuit [(1)] can detect and/or evaluate information signals and results of the detection and/or evaluation can be stored in at least one ferroelectric flip-flop [(26)], characterized in that the entire energy required for the detection, processing and storage can be generated from the information signal.

23. (amended) The use as claimed in claim 22, [characterized in that] wherein the evaluation comprises counting the arriving information signals.

24. (amended) The use as claimed in claim 23, [characterized in that] wherein the electronic circuit [(1)] can count up or count down arriving information signals.

25. (amended) The use as claimed in claim 22 [or 23], [characterized in that] wherein the electronic circuit [(1)] is used in a liquid counter.

26. (amended) A liquid counter for determining the flow of liquids through a system, [having] comprising: a sensor which can generate or generates information signals depending on a quantity of liquid flowing through the system; and an electronic circuit [(1)] as claimed in [one of] claim[s] 1 [to 14] for counting the information signals generated by the sensor; wherein the information signals are the sole energy source for the electronic circuit [(1)].

Remarks

The purpose of this Preliminary Amendment is to conform to United States Patent and Trademark Office practice and not for the purpose of patentability. No new matter has been added by way of this Preliminary Amendment.

Respectfully submitted,

INFINEON TECHNOLOGIES, AG
By its attorneys
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Description

ELECTRONIC CIRCUIT FOR A METHOD FOR STORING INFORMATION WITH FERROELECTRIC FLIP-FLOPS

The present invention relates to electronic circuits with ferroelectric flip-flops which can use arriving signals as the sole energy source, a liquid counter based on such an electronic circuit, a method for storing information contained in signals, and also the use of ferroelectric flip-flops for electronic circuits.

In conventional electronic circuits for processing signals, for example counting pulses, a supply voltage is required which supplies the logic modules. This supply voltage is supplied for example by a battery, such as a lithium battery. A battery considerably increases the production and operating costs of an apparatus which uses the circuit, and, moreover, has to be replaced at regular intervals. If results of a signal evaluation are to remain stored even when the operating voltage fails, a nonvolatile memory, for example EEPROM or FLASH-EPROM, is additionally required. Such electrically erasable memory cells require high voltages of minus 12 and plus 16 volts, respectively, for programming and for erasing, which have to be generated from the battery voltage by charge pumps. The relatively poor efficiency in high-voltage generation leads to a high power loss. Furthermore, EEPROM memories have a service life which is limited by the number of reprogramming processes. This is disadvantageous particularly in the case of counting circuits, where the so-called "Least Significant Bit" (the bit which is least significant or the smallest position of the counter) has to be reprogrammed for

each counting pulse that arrives.

Particularly in the case of apparatuses which are intended to be in operation over relatively long periods of time and/or at remote sites of use, the dependence on a supply voltage leads, moreover, to a significantly increased outlay on maintenance, since maintenance personnel have to go to the apparatuses especially for the purpose of exchanging the battery or monitoring the battery.

The use of a supply voltage generated from the electricity supply system is likewise associated with a high outlay and, in the case of remote sites, is in some instances not practicable at all. In the event of system failures, moreover, it may lead to incorrect counting results.

On account of the abovementioned disadvantages, however, there is a need to realize circuits which can operate as far as possible independently of the various voltage supplies mentioned above.

Consequently, the present invention is based on the object of providing a signal-processing and/or information-storing circuit which can be operated autonomously of external power supplies.

The present invention achieves this object by the provision of an electronic circuit in accordance with the independent patent Claim 1, a method for information storage in accordance with the independent patent Claim 16, the use of ferroelectric flip-flops for electronic circuits in accordance with the independent patent Claim 22, and the liquid counter in accordance with the independent patent Claim 26. Further advantageous configurations, details and

aspects of the present invention emerge from the dependent patent Claims, the description and the accompanying drawings.

In the analysis of signal-processing circuits and the signal-generating sensors assigned thereto, it has now been found that although the energy inherent in the signals does not suffice to be able to operate EEPROM memories, this energy nonetheless still amounts to 30nJ in the case of a typical pulse wire sensor. It has unexpectedly been found that this quantity of energy suffices to operate circuits if special flip-flops with implemented ferroelectric storage capacitances, so-called ferro-flip-flops, are used.

The present invention is therefore directed at an electronic circuit, having

an input for inputting at least one information signal;
an energy means for converting energy contained in the at least one information signal into a voltage supply;
a control means for generating at least one switch-on control signal when an information signal arrives; and
a signal processing means for storing an information item represented by the at least one information signal and/or for evaluating an information item represented by the at least one information signal and storing the secondary information obtained through the evaluation by means of at least one ferroelectric flip-flop;
wherein the signal processing means can be activated by the at least one switch-on control signal for the purpose of evaluation and/or storage;
and wherein, during the evaluation and/or storage, the at least one information signal may be or is the sole energy source for the electronic circuit.

The electronic circuit according to the invention can

thus also be provided with an external voltage supply. What is crucial, however, is that it does not rely on the latter for the information signal acquisition operation. Even in the event of a power failure, the electronic circuit according to the invention can continue to carry out its function. With regard to the power supply, the electronic circuit can thus be understood as a fail safe circuit. In particular embodiments and particularly preferred embodiments of the present invention, however, the electronic circuit is not actually provided with an external power supply, in so far as the latter is not connected for the read-out of the stored information.

The ferroelectric flip-flops used according to the invention will be described in detail further below. In principle, they have the same structure as conventional flip-flops, that is to say they have, in particular a SET and a RESET input, and also a QB and Q output and NAND or NOR gates for the circuit logic. However, they are additionally provided with ferroelectric capacitors which enable them to store the logic state of the flip-flop when the voltage supply is disconnected and to reestablish the stored state when the voltage supply is switched on. For storing or reestablishing the state of the ferroelectric flip-flop, control signals are given in a temporally exact defined sequence (see below). Nonvolatile memories based on ferroelectric capacitors can be operated at low voltages and require only about a hundredth of the energy of EEPROM memories. In the case of the electronic circuit according to the invention, therefore, it is possible for the energy (10nJ to 100nJ) required for operating a customary circuit to be drawn solely from the arriving pulse or the arriving pulses.

Thus, according to the invention, the control means

must be able to generate one or more control signals in a temporally controlled sequence and feed them to the signal processing means. This aim can be achieved in a simple manner using circuits and methods, respectively, known to persons skilled in the art. By way of example, different temporally staggered signals can be achieved by means of a bandgap difference circuit with a comparator circuit.

In the sense of the present invention, evaluation is to be understood as any interpretation of an information signal that has arrived by the signal processing means, for example the ascertainment of a time interval with respect to a preceding information signal, the logical combination via AND, OR, NAND, and NOR of different information signals, the counting up and down of information signals that arrive successively, and the toggling between on and off for successive arrivals of information signals, and any other conceivable interpretation of arriving information signals. In the sense of the present invention, a represented information item is to be understood to be any meaning which can be attributed to the input of an information signal in the temporal progression in its specific instance and in its relationship with other information signals.

The arriving information signals may have been generated by a customary sensor, for example. These are preferably sensors which generate a signal with a suitable voltage and with a sufficient energy content to be able to operate the circuit according to the invention. By way of example, inductive or piezoelectric sensors can be used. One possibility for a sensor that can be used is a pulse wire sensor, in which an external magnetic field, for example from a rotor provided with magnets, acts on a composite wire

and generates therein an electrical pulse which is then available as information signal. In this case, the entire energy that is required is drawn from the magnetic field, so that an external energy supply is also not necessary for the sensor.

The electronic circuit according to the invention is preferably characterized in that the control means can generate at least one switch-off control signal after a predetermined time has elapsed after the at least one information signal arrives and/or when the energy converted from the at least one information signal is exhausted, wherein the signal processing means can be caused or is caused to effect a storage and to effect deactivation by the at least one switch-off control signal.

It is understood that a switch-off control signal is to be generated after time has elapsed only when, after the arrival of an information signal, no further information signal has arrived. The elapsing of a predetermined time thus always relates to the elapsing after the inputting of the last information signal, if a plurality of information signals have arrived successively. If the switch-off control signal is generated when the existing energy is exhausted, it is necessary to provide a circuit in the control means which can reliably ascertain that said energy is exhausted. By way of example, it is possible to use a circuit which can detect a possible voltage drop.

Preferably, the information stored in the at least one ferroelectric flip-flop can be converted into at least one output signal by the signal processing means, wherein in this case the electronic circuit furthermore has at least one output for outputting the at least one output signal. In this way, the information stored in

the circuit can be read out again by a suitable read-out means.

The electronic circuit may furthermore have a display means for displaying the information stored in the at least one ferroelectric flip-flop. Such an additional display means is possible when sufficient energy for operating it can be obtained from the information signal. A display means enables the information stored in the at least one flip-flop to be read at any time.

Preferably, the display means is concomitantly supplied by the voltage supply generated by the energy means. However, it is also possible to configure the display means in such a way that it requires an external voltage supply. In this case, with autonomous operation of the electronic circuit, before the reading of the display means, an external voltage supply must first be connected. If the electronic circuit has an external voltage supply anyway, for example in the case of the above-described area of use of fail-safe circuits, such an external connection will generally not be necessary.

In order to keep the energy consumption of the display means as low as possible, an LCD display will preferably display the information. However, it is also possible to use other displays if they have a sufficiently low energy consumption. In order to ensure a coordinated transfer of information contained in the ferroelectric capacitors of the ferroelectric flip-flops to the logic gates of the ferroelectric flip-flop, the switch-on control signal preferably has the following signals:

an activation signal for activating precharge transistors of the at least one ferroelectric flip-flop; a transfer signal for transferring the

information contained in ferroelectric capacitors of the at least one ferroelectric flip-flop onto internal data lines of the at least one ferroelectric flip-flop; and a current switching signal for switching on the voltage supply of the signal processing means.

In order to ensure that the information contained in the at least one ferroelectric flip-flop is written back in the event of a voltage drop, the switch-off control signal preferably has the following signals:
a transfer end signal;
an activation signal for activating precharge transistors of the at least one ferroelectric flip-flop; and
a current switch-off signal for switching off the voltage supply of the signal processing means.

These different signals are transferred from the control means to the signal processing means preferably by virtue of the fact that signal lines for each of the switch-on signals and switch-off signals lead from the control means to the signal processing means. By way of example, moreover, for the transfer signal and the transfer end signal, a common transfer signal line may lead from the control means to the signal processing means, in which case the transfer signal may consist in the application of a voltage to the common transfer signal line and the transfer end signal may consist in the disconnection of the voltage on the common transfer signal line.

Equally, for the current switching signal and current switch-off signal, a common current signal line may lead from the control means to the signal processing means, wherein the current switching signal consists in the application of a voltage to the common current signal line and the current switch-off signal consists

in the disconnection of the voltage on the common current signal line.

Since it is generally very easy to realize counting circuits using flip-flops, it is a preferred embodiment of the present invention that the signal processing circuit is a counting circuit for evaluating a plurality of information signals, which arrive successively or simultaneously, by counting the information signals that have arrived. In this case, it is thus possible for one or more information signal lines to be served simultaneously, provided that the circuit is able to do this. What is then involved is an input signal bus.

The counting circuit comprises, for example, a plurality of cascaded edge-controlled ferroelectric flip-flops, in which the at least one information signal is input into the clock input of the first ferroelectric flip-flop of the plurality of cascaded ferroelectric flip-flops and the output of each of the ferroelectric flip-flops, except for the last, is in each case also connected to the clock input of the ferroelectric flip-flop connected downstream.

What is thus involved in this case is a customary counter circuit arrangement of flip-flops in which, however, ferroelectric flip-flops are used instead of the conventionally used flip-flops.

The invention is also directed at a method for storing information contained in information signals. With regard to the advantages, effects and actions of the method, the statements made above are hereby incorporated by reference in their entirety.

The invention is also directed at a method for storing

information represented by at least one information signal or information obtained through evaluation of the at least one information signal in at least one ferroelectric flip-flop in a signal processing means, having the following steps:

A: generating at least one switch-on control signal from an information signal that has arrived, and generating a voltage supply from energy contained in the at least one information signal;

B: activating the signal processing means by the switch-on control signal and applying the voltage supply to the signal processing means;

C: storing an information item represented by the at least one information signal and/or evaluating an information item represented by the at least one information signal and storing the secondary information obtained through the evaluation by means of at least one ferroelectric flip-flop;

D: generating a switch-off control signal after a predetermined time has elapsed after the at least one information signal arrives and/or when the energy converted from the at least one information signal is exhausted; and

E: deactivating the signal processing means by the switch-off control signal.

Therefore, in the case of the method according to the invention, too, two possibilities are available for determining the instant at which a switch-off control signal is generated, namely, on the one hand, once again the simple measurement of a time that has elapsed after the arrival of an information signal, and, on the other hand, the measurement of the energy that is still available and has been obtained from the information signal. This last can be determined, for example, by

means of a voltage drop. In this case, too, it is understood that, in the event of the successive arrival of a plurality of information signals, it is desirable for the method not to have the result that, independently of the arrival of further information signals, in a manner governed by the switch-off, these can no longer be detected. Rather, care should be taken in this case, too, to ensure that the time that has elapsed since the last information signal that arrived is measured in each case and that the time measurement starts anew when a new information signal arrives.

In the sense of the method according to the invention, deactivation of the signal processing means is in this case to be understood to mean that the switching-logic states contained in the ferroelectric flip-flops are written back to the ferroelectric capacitors in a controlled manner in order to have the content reliably stored in the event of the final disconnection of the voltage supply.

Step B of the method according to the invention may preferably have the following sub-steps:

B1: activating precharge transistors of the at least one ferroelectric flip-flop by applying a voltage;
B2: deactivating the precharge transistors of the at least one ferroelectric flip-flop by disconnecting the voltage;
B3: applying a voltage to ferroelectric capacitors of the at least one ferroelectric flip-flop for transferring the information stored in the ferroelectric capacitors to logic gates of the at least one ferroelectric flip-flop; and
B4: activating the voltage supply of the logic gates of the at least one ferroelectric flip-flop.

By this sequence of signals which are based on voltage changes, a reliable transfer of the information already stored beforehand to the logic gates of the ferroelectric flip-flop is achieved.

It is also the case in the context of the disconnection of the signal processing means that a specific order of steps is preferably adhered to. Therefore, step E may preferably have the following sub-steps:

E1: disconnecting a voltage present across ferroelectric capacitors of the at least one ferroelectric flip-flop;
E2: deactivating the voltage supply of the logic gates of the at least one ferroelectric flip-flop;
E3: activating precharge transistors of the at least one ferroelectric flip-flop by applying a voltage; and
E4: deactivating the precharge transistors of the at least one ferroelectric flip-flop by disconnecting the voltage.

By virtue of these steps, the opposite process is carried out, in which the levels present at the logic gates are written back to the ferroelectric capacitors as information to be stored.

Preferably, the electronic circuit contains a plurality of ferroelectric flip-flops, wherein the evaluation in step C comprises a summation of the value represented by the information signal and a value already stored in the ferroelectric flip-flops.

Preferably, the summation is effected by means of a counting operation in which the plurality of ferroelectric flip-flops are cascaded in a counter arrangement and an arriving information signal increments or decrements a counter reading of the

counter arrangement by the value 1.

Such incrementing or decrementing by the value 1 is appropriate, of course, only if there is merely one input for an information signal. If it is possible for a plurality of information signals to arrive simultaneously or successively via different inputs, the value must be incremented or decremented accordingly.

By way of example, the information stored in the at least one ferroelectric flip-flop can be converted into at least one output signal and be output from the electronic circuit. This additional method step ensures that the information obtained through the information signals can also actually be made available to a user.

The invention is likewise directed at the use of ferroelectric flip-flops. With regard to the effects, advantages and actions of such a use, the statements made above are hereby incorporated by reference in their entirety.

The invention is accordingly directed at the use of ferroelectric flip-flops for electronic circuits, wherein the electronic circuit can detect and/or evaluate information signals and results of the detection and/or evaluation can be stored in at least one ferroelectric flip-flop, this use being characterized in that the entire energy required for the detection, processing and storage can be generated from the information signal.

In this case, the evaluation may comprise counting the arriving information signals. In this case, the electronic circuit can count up or count down the arriving information signals.

Particular preference is attached to a use which is characterized in that the electronic circuit is used in a liquid counter. In the present invention, a liquid counter is understood to be a device which is able to determine the flow of a liquid thorough a cross section, for example a pipe or a channel, and to add up the total quantity of liquid which has flowed through the cross section starting from a start instant. Liquid counters often have to remain at the installation site for long periods of time without being able to be provided with an external power supply. Thus, this is a particularly interesting application example for the present invention, since previous electrical liquid counters require batteries to be exchanged.

Accordingly, the invention is finally also directed at a liquid counter for determining the flow of liquids through a system, having: a sensor which can generate or generates information signals depending on a quantity of liquid flowing through the system; and an electronic circuit which is constructed according to the invention and serves for counting the information signals generated by the sensor; wherein the information signals are the sole energy source for the electronic circuit.

The invention will be explained below using general exemplary embodiments and be illustrated in detail, reference being made to the accompanying drawings, in which the following is illustrated:

Figure 1 shows a diagrammatic illustration of an embodiment of the electronic circuit according to the present invention;

Figure 2 shows a further embodiment of an electronic

circuit according to the present invention, in which a display unit is additionally provided;

Figure 3 shows a ferroelectric flip-flop which is used in the following invention, with only NOR gates;

Figure 4 shows a further ferroelectric flip-flop which can be used in the invention, with NAND gates;

Figure 5 shows a less abstract circuit diagram of the ferroelectric flip-flop illustrated in Figure 3, for use in the present invention;

Figure 6 shows a ferroelectric flip-flop which is edge-controlled by additional logic gates and forms a divider;

Figure 7 shows a counter circuit with the edge-controlled flip-flops shown in Figure 6;

Figures 8A and 8B show an exemplary temporal progression of the control and information signals and of the voltage supply in the case of an electronic circuit according to the invention.

Figure 1 shows the diagrammatic illustration of a possible embodiment of an electronic circuit according to the present invention. The electronic circuit 1 firstly has an input 5, via which an information signal can pass into the electronic circuit 1 by means of a signal line. The information signal is fed to the various functional units on a signal distributor 7. An energy means 2 receives the information signal in order

to be able to generate from it a voltage supply, if appropriate even with a plurality of different voltages, depending on the requirements of the electronic circuit 1.

A control means 3 likewise receives the information signal in order thus to be put in the position of being able to produce control signals or at least one control signal in a temporally controlled sequence.

The voltages used for the voltage supply and the various control signals are dimensioned according to the type of circuit layout used and the components used, but likewise according to the voltage of the arriving information signals. The latter is typically determined from the voltage generated by a sensor or something similar which generates the information signals.

Whereas energy means 2 and control means 3 are illustrated as separate units in the illustration in Figure 1, it is equally possible to combine both means to form a functional and operative unit. In actual fact, for reasons of simplification and saving costs, in practice, often just a single circuit will be used which is able both to generate a voltage supply and to generate suitable control signals.

The voltage supply made available by the energy means 2 is fed via the voltage supply bus 9 both to the control means 3 and to the signal processing means 4. The latter furthermore receives the information signal via the signal distributor 7 and, when an information signal arrives, likewise the control signal via at least one control signal line or a control signal bus 8. Thus, the basic principle of the circuit according to the invention is that the information signal which

has arrived at the input 5 is split and fed to different uses. On the one hand, part of the energy contained therein is used for a voltage supply; on the other hand, the instant of arrival is also used in order to make available control signals for activation and deactivation of the actual evaluation unit, and, finally, the information signal is fed to the actual signal processing unit, where it is either only stored or evaluated and is then stored in the ferroelectric flip-flops for example in the event of a power failure or after time has elapsed. The signal processing means 4 can make available a wide variety of types of processing or evaluation of information signals. Typical applications encompass a wide variety of types of counters, such as, for example, asynchronous or synchronous binary counters, counters with a switchable counting device, counters with up and down input, BCD counters and preselection counters and also shift registers. Other circuit logic arrangements can also be realized, for example those in which more than one information signal arrives at the same time and in which logical combinations are produced between the information signals, whose result can finally be stored in a ferroelectric flip-flop, even in the event of a power failure.

A prerequisite for the operation of the electronic circuit 1 according to the invention is that the information signals arriving at the input 6 have a sufficient energy content to be able to supply the electronic circuit 1 with energy. Such quantities of energy, which are of the order of magnitude of between 10 and 100nJ, are supplied for example by active converters such as, for example, inductive or piezoelectric sensors. Since there is thus sufficient energy available, an additional voltage supply is no longer required at least for the actual counting

operation.

Figure 1 likewise illustrates a signal output by means of which the information stored in the ferroelectric flip-flops or, in the event of lengthy operation, the information that is in each case currently present at the logic gates in the ferroelectric flip-flops can be read out. In the simplest case, this is a single signal line which is routed out at the output 6. If only a binary representation, that is to say 1 or 0 is stored as information in the ferroelectric flip-flops, it suffices simply to read out the latter. However, if a plurality of bit information items are buffer-stored in the signal-processing means 4 by means of a plurality of ferroelectric flip-flops, it may be necessary either to route a plurality of signal lines toward the outside, which simultaneously pass the outputs of the various ferroelectric flip-flops toward the outside, or to provide an additional circuit which, in a temporal sequence, can output the individual bits of the various ferroelectric flip-flops successively via the output 6.

Figure 2 shows a modification of a further exemplary embodiment of an electronic circuit according to the present invention, in which, in comparison with Figure 1, a display means 10 with an LCD display 11, for example, has also been added. In the exemplary embodiment illustrated in Figure 2, the display means 10 is likewise supplied with energy by the voltage supply bus 9 and the information stored in the ferroelectric flip-flops of the signal processing means is likewise output to the display means 10. In this case, the display means 10 can either be connected directly to the outputs of the ferroelectric flip-flops or, as illustrated in Figure 2, being concomitantly served by the same output signal line which also supplies information at the output 6.

The ferroelectric flip-flops used in the electronic circuit according to the invention and in the method according to the invention will be described in more detail below.

Figure 3 shows a diagrammatic illustration of a ferroelectric flip-flop. The latter has the elements that are known in conventional flip-flops, in particular two logic gates, in this case NOR gates 12,13, which can be driven in each case via an input SET and RESET, respectively, and also two inverters 20,21, which are connected to the NOR gates 12,13 via internal data lines QBint 22 and Qint 23 and can output the inverted results of the logic gates via the outputs Q and QB, respectively. Over and above this known construction, however, ferroelectric flip-flops have further specific elements. The latter are, firstly, the characteristic ferroelectric capacitors 14,15, which can be supplied with voltage via a line PL. In addition there are the precharge transistors 18,19, which can be activated via the line PRECH and can be supplied with voltage via the line VPRECH. The further capacitances 16,17 may optionally be provided. The NOR gates of the two circuits are designed symmetrically, so that the state assumed upon switch-on depends on the charge on the networks Qint23 and QBint 22, if the inputs SET and RESET are not active at this point in time. The charge on the networks Qint23 and QBint 22 is read from the ferro-capacitors 14,15 before the switch-on of the logic gates and corresponds to the last state assumed by the flip-flop before the last switch-off. The read-out from the ferroelectric capacitors is effected according to the scheme outlined below.

Firstly, the internal data lines 22,23 are precharged to a specific voltage VPRECH, for example 0 volts, via

the precharge transistors 18,19 and the associated control signal PRECH. In order to achieve this, the NOR gates must not yet be supplied with operating voltage. Afterward, the transistors 18,19 are turned off again. As a result, the networks Qint23 and QBint22 are at high impedance.

A signal PL, which until now has been kept at the same potential as VPRECH, is then raised to a specific voltage. Charge equalization is then effected by means of the capacitive voltage dividers produced from the ferroelectric capacitors and the capacitances 16,17 of the networks Qint23 and QBint22. The capacitances 16,17 may either only consist of component input or wiring capacitances or additionally be increased by capacitances that are actually realized. In order to ensure that the value of these capacitances is independent of the circuitry at the output of the ferroelectric flip-flops, the internal data lines Qint23 and QBint22 are decoupled from the actual outputs of the circuit Q and QB by two inverters 20,21. However, if the switching mechanism in which the ferroelectric flip-flop is used is known, the output inverters can possibly be omitted. Depending on the stored state of the ferroelectric capacitors, the potential of one internal data line (Qint23 or QBint22) after the charge equalization is now greater than the potential of the other data lines. The potential of the input PL can now either be kept at the higher potential or be reduced to VPRECH again.

The voltage supply of the NOR gates is now switched on, so that the flip-flop latches to one of the two possible states, depending on what voltages are present on the internal data lines Qint23 and QBint22. What is important in this case is that the inputs of the NOR gates are furthermore not active, that is to say that

SET and RESET must be at logic LOW. After the switch-on and switch-off of this operation, the ferroelectric flip-flops can be operated like customary flip-flops.

Figure 4 shows a further ferroelectric flip-flop for use in the present invention, which corresponds to the flip-flop shown in Figure 3, but NAND gates 24,25 are used instead of the NOR gates 12,13. The internal data lines are correspondingly changed.

In an illustration which is configured more concretely but is still slightly diagrammatic, Figure 5 shows a more concrete embodiment of the ferroelectric flip-flop shown generally in Figure 3 for use with the present invention. The two NOR gates 12,13 and the two inverters 20,21 are in this case depicted with their transistors that are used in each case.

The text below describes how the ferroelectric flip-flop illustrated in Figure 5 is made ready for operation. Firstly, the two precharge transistors 18,19 are activated by means of the signal PRECH. Afterward, the voltage supply VDD is raised to a suitable value, for example 3 volts. The precharge transistors 18,19 are then turned up and the voltage at the input PL is increased to a value corresponding to VDD, for example 3 volts, so that the two transfer switching transistors 30,31 are activated, which causes the information contained in the ferroelectric capacitors 14,15 to be transferred onto the internal data lines 22,23. At this point in time, then, the ferroelectric capacitors and the inverters are supplied with current. Only afterward is the supply voltage of the two NOR gates 12,13 switched on by the signals NSET and PSET being raised to the voltage used, for example 3 volts, which causes the two logic switching transistors 32,33 to be activated and a voltage between VDD and VSS then to be

present at the transistors.

Figure 5 furthermore shows a transistor for the logic gates 28, which pulls the positive voltage supply of the NOR gates 12,13 to a fixed potential VSS if a voltage is applied at the signal PRECH.

The ferroelectric flip-flop shown in Figure 5 is deactivated in the reverse order. Firstly, the signal PL is turned off. The voltage supply of the NOR gates 12,13 is then disconnected by turning off NSET. Afterward, the precharge transistors 18,19 are activated by a signal at PRECH, in order to avoid interference pulses on the ferroelectric capacitors. Finally, the supply voltage as such is disconnected and lastly the signal PRECH of the precharge transistors 18,19.

The ferroelectric flip-flops outlined above can be used in manifold ways in the electronic circuits according to the present invention and in the method of the present invention. The text below will describe a concrete application which realizes a counter comprising a plurality of cascaded ferroelectric flip-flops. It is understood, however, that other circuit arrangements can also be realized in the context of the present invention, for example ones in which a plurality of arriving information signals can be simultaneously combined with one another in a specific manner.

Figure 6 firstly shows how a ferroelectric flip-flop 26, as illustrated in Figure 5, is provided with an additional logic circuit in order to make it into an edge-controlled flip-flop which simultaneously fulfils a dividing function, that is to say changes the state at one of the outputs Q,QB upon every falling edge of

an information signal. The circuit 34 represents a dividing unit which, however, simultaneously represents a special instance of a flip-flop, as is known to the person skilled in the art.

Two NOR gates 35,36 and two NAND gates 37,38 are in each case connected to an input for the information signal, said input being designated by CLK. The designation CLK therefore shows that what is involved in this case is also a clock-controllable flip-flop in which a clock signal (CLOCK) can then be applied to this input. The two inputs NSET and PSET of the ferroelectric flip-flop 26, which are already known from Figure 5, are combined by means of an inverter in the circuit arrangement of Figure 6, so that both are driven by a common input signal, which is again designated as NSET. A further input ENABLE is provided in the circuit arrangement of Figure 6, which input must be activated in order that an information signal arriving at the input CLK is forwarded by the NOR gates 35,36 to the inputs SET and RESET, respectively, of the ferroelectric flip-flop 26.

Finally, Figure 7 shows the integration of a plurality of these dividing devices 34 in a counter arrangement. As can be discerned here, the information signal arriving via the input CLK is fed only to the first dividing circuit 34 in the sequence of dividing circuits. The output Q of the ferroelectric flip-flop is passed on to the input CLK of the next ferroelectric flip-flop or of the next dividing unit 34. The lines for the control signals PRECH, PL, NSET and, finally, the ENABLE added in Figure 6 (input is CLKEN here) correspond to Figures 5 and 6.

The state of the first edge-controlled ferroelectric flip-flop 34 changes in each case with the edge of an

information signal arriving at CLK. The same occurs with the second edge-controlled ferroelectric flip-flop 34 in the arrangement, which receives signals from the output Q of the first edge-controlled ferroelectric flip-flop at the input CLK. This means that the state of the output Q at the second edge-controlled ferroelectric flip-flop 34 changes only for every second information signal. Consequently, a counting circuit is implemented in which the left-hand edge-controlled ferroelectric flip-flop represents the less significant bit; the one furthest on the right represents the most significant bit. In this case, the number of cascaded flip-flops determines the maximum number of arriving information signals. With eight cascaded ferroelectric flip-flops 34, it is possible, for example, to represent the range of decimal numbers between 0 and 255 (corresponding to 0000 0000 to 1111 1111 binary).

The temporal sequence of a counting operation by the circuit shown in Figure 7 will now be clarified with reference to the graphics in Figure 8. The graphics show two signal acquisition cycles that proceed one after the other. Figure 8 shows the temporal profile of the voltages present at various inputs and outputs of the circuit in their temporal profile. The time sequence in ns is represented on the abscissa, while the voltages of the signals that are respectively present are represented on the various ordinates. By being arranged one below the other it is possible to assess the temporal sequence of the signals relative to one another.

As explained above, firstly the voltage is applied to the input PRECH in order to activate the precharge transistors 18,19. The signal PRECH is formed by the control means 3. Immediately afterward, the operating

voltage VDD is applied to the entire system. This voltage is generated by the energy means 2. As illustrated in Figure 8B, this has the result that a voltage is likewise at the respective outputs Q0 to 2 of the three ferroelectric flip-flops 34 shown by way of example here. Immediately after the operating voltage VDD has been switched on, the voltage at the input PRECH is disconnected.

The control means 3 then generates a voltage at the input PL of the ferroelectric flip-flops, which leads to the deactivation of the transfer switching transistors 30,31 and thus to the transferring of the information stored in the ferroelectric capacitors 14,15 onto the internal data lines 22,23. As shown in Figure 8B, at this instant the outputs of the three ferroelectric flip-flops shown by way of example assume the defined level states, that is to say 0 in this case, since as yet no information is stored in the ferroelectric flip-flops 26. Afterward, the control means 3 generates a voltage at the input NSET (and also at the input PSET in some embodiments), which leads to the activation of the logic switching transistors 33 (and possibly 32), with the result that the operating voltage of the NOR gates 12,13, or of the NAND gates 24,25 if NAND gates are used, is switched on.

In the present experimental application of an electronic circuit according to the invention, no individually arriving information signals are used. Rather, as shown in Figure 8B, bottom line, a clock signal is generated, which is applied to the input CLK. The ferroelectric flip-flops or dividers 34 (see Figure 6) used in Figure 7 have an additional input which is required in order to enable a transfer of the information signal present at the input CLK to the inputs of the ferroelectric flip-flop 26, namely the

input ENABLE. Only after the control means 3 applies a voltage to the input ENABLE (see Figure 8B, bottom, solid signal line) does the occurrence of the information signals applied to the input CLK lead to a reaction at the outputs of the ferroelectric flip-flops or dividers 34. With the falling edge of the first information signal arriving after the switch-on of the ENABLE input, the output signal changes from level 0 to level Logic 1 at the output of the first of the cascaded ferroelectric flip-flops. After the fall of the second arriving information signal, the level changes to Logic 0 again, whereupon the level at the output of the ferroelectric flip-flop connected downstream goes to Logic 1. In the temporal progression of the experiment, a turn-off operation is then simulated, as would be effected, in an electronic circuit according to the invention, by the control means after a specific time has elapsed after the arrival of a last information signal or in the event of the expected fall in the voltage supply on account of energy deficiency.

This fall is only simulated in the case of the experiment shown, since the clock signal continues to be present at the input CLK.

In order to deactivate the ferroelectric flip-flops according to the invention, firstly the ENABLE and PL signals are turned off. Afterward, the voltage supply of the logic gates is disconnected by turning off the signal NSET. What is achieved as a result is that the information contained in the three ferroelectric flip-flops is correctly written back to the ferroelectric capacitors. The precharge transistors 18,19 are then momentarily activated, the entire voltage supply is disconnected and, finally, the precharge transistors are deactivated.

Afterward, a further signal acquisition cycle is initiated in the experiment. The sequence corresponds to the above-described first activation of the electronic circuit. As shown in Figure 8B, however, the information of the individual ferroelectric flip-flops which is stored in the ferroelectric capacitors 14,15 is written back to the logic gates, so that a level of Logic 1 is established in accordance with the state prior to the last disconnection at the outputs of the first and second of the series of ferroelectric flip-flops. The information represented by the three ferroelectric flip-flops thus corresponds to the binary value 011, that is to say a decimal numerical value of 3. After the ENABLE signal has in turn been switched on, three information signals are then again counted, so that, at the end of this information signal acquisition phase, the three ferroelectric flip-flops contain the binary value 110 (corresponding to the decimal numerical value 6). Finally, Figure 8 shows yet another deactivation sequence, which again has the result that said information present at the outputs of the ferroelectric flip-flops 26 is transferred into the respective ferroelectric capacitors 14,15.

The experimental signal acquisition operation shown in Figure 8 was able to show that it is actually possible with the electronic circuit according to the invention to buffer-store the information contained in the ferroelectric flip-flops and to re-establish it upon the reoccurrence of signals or of voltage.

Patent Claims

1. Electronic circuit (1), having

an input (5) for inputting at least one information signal;

an energy means (2) for converting energy contained in the at least one information signal into a voltage supply;

a control means (3) for generating at least one switch-on control signal when an information signal arrives; and

a signal processing means (4) for storing an information item represented by the at least one information signal and/or for evaluating an information item represented by the at least one information signal and storing the secondary information obtained through the evaluation by means of at least one ferroelectric flip-flop (26);

wherein the signal processing means (4) can be activated by the at least one switch-on control signal for the purpose of evaluation and/or storage;

and wherein, during the evaluation and/or storage, the at least one information signal may be or is the sole energy source for the electronic circuit (1).

2. The electronic circuit as claimed in claim 1, characterized
in that the control means (3) can generate at least one switch-off control signal after a predetermined time has elapsed after the at least one information signal

arrives and/or when the energy converted from the at least one information signal is exhausted,

wherein the signal processing means (4) can be caused or is caused to effect a storage and to effect deactivation by the at least one switch-off control signal.

3. The electronic circuit (1) as claimed in claim 1 or 2, characterized in that the information stored in the at least one ferroelectric flip-flop (26) can be converted into at least one output signal by the signal processing means (4) and the electronic circuit (1) furthermore has at least one output (6) for outputting the at least one output signal.

4. The electronic circuits (1) as claimed in one of claims 1 to 3, characterized in that the electronic circuit furthermore has a display means (10) for displaying the information stored in the at least one ferroelectric flip-flop (26).

5. The electronic circuit (1) as claimed in claim 4, characterized
in that the display means (10) is concomitantly supplied by the voltage supply generated by the energy means (2).

6. The electronic circuit (1) as claimed in claim 4 or 5, characterized
in that the display means (10) has an LCD display (11).

7. The electronic circuit (1) as claimed in one of claims 3 to 6, characterized
in that an external voltage supply and external control means can be connected for the outputting of the information stored in the at least one ferroelectric

flip-flop (26) by the signal processing means (4).

8. The electronic circuit (1) as claimed in one of claims 1 to 7, characterized
in that the at least one switch-on control signal has the following signals:

an activation signal (PRECH) for activating precharge transistors (18,19) of the at least one ferroelectric flip-flop (26);

a transfer signal (PLN) for transferring the information contained in ferroelectric capacitors (14,15) of the at least one ferroelectric flip-flop (26) onto internal data lines (22,23) of the at least one ferroelectric flip-flop (26); and

a current switching signal (NSET) for switching on the voltage supply of the signal processing means (4).

9. The electronic circuit (1) as claimed in one of claims 2 to 8, characterized
in that the at least one switch-off control signal has the following signals:

a transfer end signal (PLN);

an activation signal (PRECH) for activating precharge transistors (18,19) of the at least one ferroelectric flip-flop (26); and

a current switch-off signal (NSET) for switching off the voltage supply of the signal processing means (4).

10. The electronic circuit (1) as claimed in claim 8 or 9, characterized
in that signal lines (8) for each of the switch-on

signals lead from the control means (3) to the signal processing means (4).

11. The electronic circuit (1) as claimed in claim 9 or 10, characterized
in that signal lines (8) for each of the switch-off signals lead from the control means (3) to the signal processing means (4).

12. The electronic circuit (1) as claimed in claim 11, characterized
in that, for the transfer signal and the transfer end signal, a common transfer signal line leads from the control means (3) to the signal processing means (4), the transfer signal consists in the application of a voltage to the common transfer signal line and the transfer end signal consists in the disconnection of the voltage on the common transfer signal line.

13. The electronic circuit (1) as claimed in claim 11 or 12, characterized
in that, for the current switching signal and the current switch-off signal, a common current signal line leads from the control means (3) to the signal processing means (4), the current switching signal consists in the application of a voltage to the common current signal line and the current switch-off signal consists in the disconnection of the voltage on the common current signal line.

14. The electronic circuit (1) as claimed in one of claims 1 to 13, characterized
in that the signal processing circuit (4) is a counting circuit for evaluating a plurality of information signals, which arrive successively or simultaneously, by counting the information signals that have arrived.

15. The electronic circuit (1) as claimed in claim 14, characterized
in that the counting circuit comprises a plurality of cascaded edge-controlled ferroelectric flip-flops (34), in which the at least one information signal is input into the clock input (CLK) of the first ferroelectric flip-flop (34) of the plurality of cascaded ferroelectric flip-flops (34) and the output (Q) of each of the ferroelectric flip-flops (34), except for the last, is in each case also connected to the clock input (CLK) of the ferroelectric flip-flop (34) connected downstream.

16. A method for storing information represented by at least one information signal or information obtained through evaluation of the at least one information signal in at least one ferroelectric flip-flop (26) in a signal processing means (4), having the following steps:

A: generating at least one switch-on control signal from an information signal that has arrived, and generating a voltage supply from energy contained in the at least one information signal;
B: activating the signal processing means (4) by the switch-on control signal and applying the voltage supply to the signal processing means (4);
C: storing an information item represented by the at least one information signal and/or evaluating an information item represented by the at least one information signal and storing the secondary information obtained through the evaluation by means of at least one ferroelectric flip-flop (26);
D: generating a switch-off control signal after a predetermined time has elapsed after the at least one information signal arrives and/or when the energy converted from the at least one information signal is

exhausted; and
E: deactivating the signal processing means (4) by the switch-off control signal.

17. The method as claimed in claim 16, characterized in that step B has the sub-steps:

B1: activating precharge transistors (18,19) of the at least one ferroelectric flip-flop (26) by applying a voltage:
B2: deactivating the precharge transistors (18,19) of the at least one ferroelectric flip-flop (26) by disconnecting the voltage;
B3: applying a voltage to ferroelectric capacitors (14,15) of the at least one ferroelectric flip-flop (26) for transferring the information stored in the ferroelectric capacitors (14,15) to logic gates (12,13,24,25) of the at least one ferroelectric flip-flop (26); and
B4: activating the voltage supply of the logic gates (12,13,24,25) of the at least one ferroelectric flip-flop (26).

18. The method as claimed in claim 16 or 17, characterized
in that step E has the sub-steps:
E1: disconnecting a voltage present across ferroelectric capacitors (14,15) of the at least one ferroelectric flip-flop (26);
E2: deactivating the voltage supply of the logic gates (12,13,24,25) of the at least one ferroelectric flip-flop (26);
E3: activating precharge transistors (18,19) of the at least one ferroelectric flip-flop (26) by applying a voltage; and
E4: deactivating the precharge transistors (18,19) of the at least one ferroelectric flip-flop (26) by

disconnecting the voltage.

19. The method as claimed in one of claims 16 to 18, characterized
in that the electronic circuit (1) contains a plurality of ferroelectric flip-flops (26) and the evaluation comprises a summation of the value represented by the information signal and a value already stored in the ferroelectric flip-flops (26).

20. The method as claimed in claim 19, characterized in that the summation is effected by means of a counting operation in which the plurality of ferroelectric flip-flops (26) are cascaded in a counter arrangement and an arriving information signal increments or decrements a counter reading of the counter arrangement by the value 1.

21. The method as claimed in one of claims 16 to 20, characterized
in that the information stored in the at least one ferroelectric flip-flop (26) can be converted into at least one output signal and be output from the electronic circuit (1).

22. The use of ferroelectric flip-flops (26) for electronic circuits, wherein the electronic circuit (1) can detect and/or evaluate information signals and results of the detection and/or evaluation can be stored in at least one ferroelectric flip-flop (26), characterized in that the entire energy required for the detection, processing and storage can be generated from the information signal.

23. The use as claimed in claim 22, characterized
in that the evaluation comprises counting the arriving information signals.

24. The use as claimed in claim 23, characterized in that the electronic circuit (1) can count up or count down arriving information signals.

25. The use as claimed in claim 22 or 23, characterized in that the electronic circuit (1) is used in a liquid counter.

26. A liquid counter for determining the flow of liquids through a system, having:
a sensor which can generate or generates information signals depending on a quantity of liquid flowing through the system; and
an electronic circuit (1) as claimed in one of claims 1 to 14 for counting the information signals generated by the sensor;
wherein the information signals are the sole energy source for the electronic circuit (1).

(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

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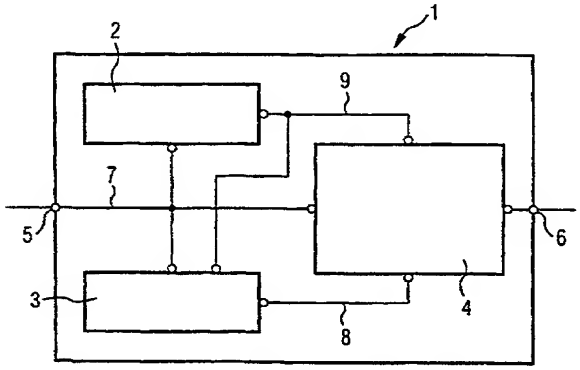
(81) Bestimmungsstaaten *(national)*: JP, US.

(84) Bestimmungsstaaten *(regional)*: europäisches Patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

[Fortsetzung auf der nächsten Seite]

(54) Title: ELECTRONIC CIRCUIT FOR A METHOD FOR STORING INFORMATION, SAID CIRCUIT COMPRISING FERROELECTRIC FLIPFLOPS

(54) Bezeichnung: ELEKTRONISCHE SCHALTUNG FÜR EIN VERFAHREN ZUR SPEICHERUNG VON INFORMATIONEN MIT FERROELEKTRISCHEN FLIPFLOPS



(57) Abstract: A supply voltage is needed in conventional electronic circuits used for processing signals, such as counting pulses. The supply voltage supplies the logic circuit components. Especially apparatuses which have to be operated over a longer period of time or/and in remote sites of use and are dependent upon a supply voltage are impaired with the dependency-related disadvantages, such as the necessity of expensive EEPROMs or significantly increased maintenance expenditure. The present invention relates to an electronic circuit which is provided with an input (5) for inputting at least one information signal, an energy means (2) for converting the energy that is present in the at least one information signal into a supply voltage, a control means (3) for generating at least one switch-on control signal when the information signal is input and a signal processing means (4) for storing information which is represented by the at least one information signal and/or for evaluating information which is represented by the at least one information signal and for storing the secondary information which is obtained by the evaluation. At least one ferroelectric flipflop (26) is used. The signal processing means (4) can be activated by the at least one switch-on control signal for evaluating and/or storing purposes. The at least one information signal can be or is the only energy source for the electronic circuit (1) during the evaluation and/or storing process.

[Fortsetzung auf der nächsten Seite]

WO 01/15323 A1

FIG 1

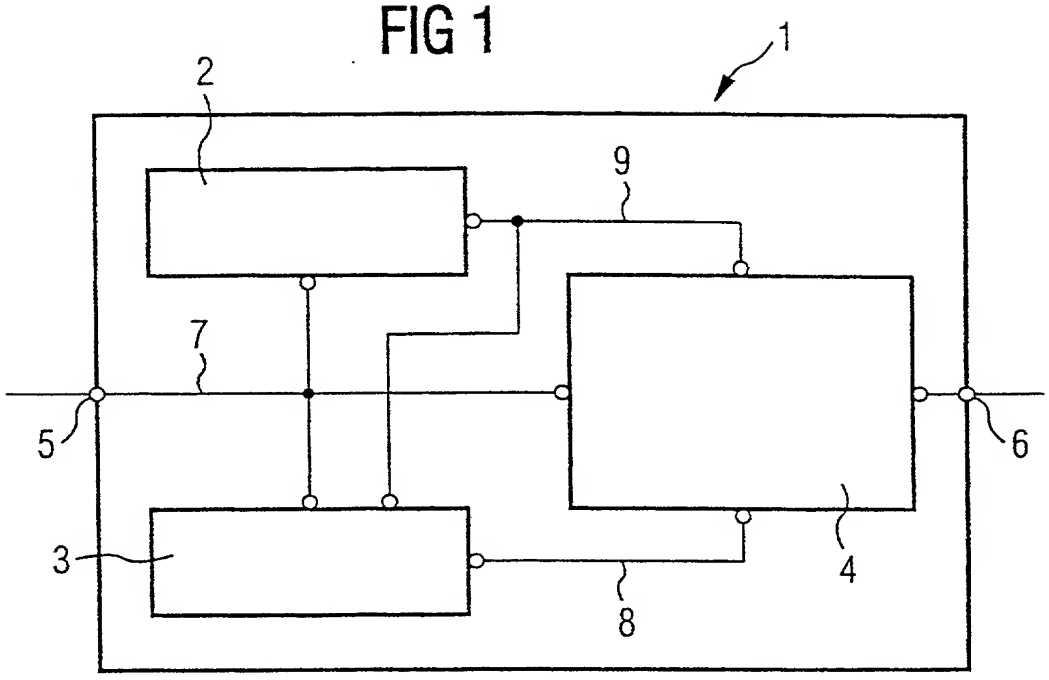


FIG 2

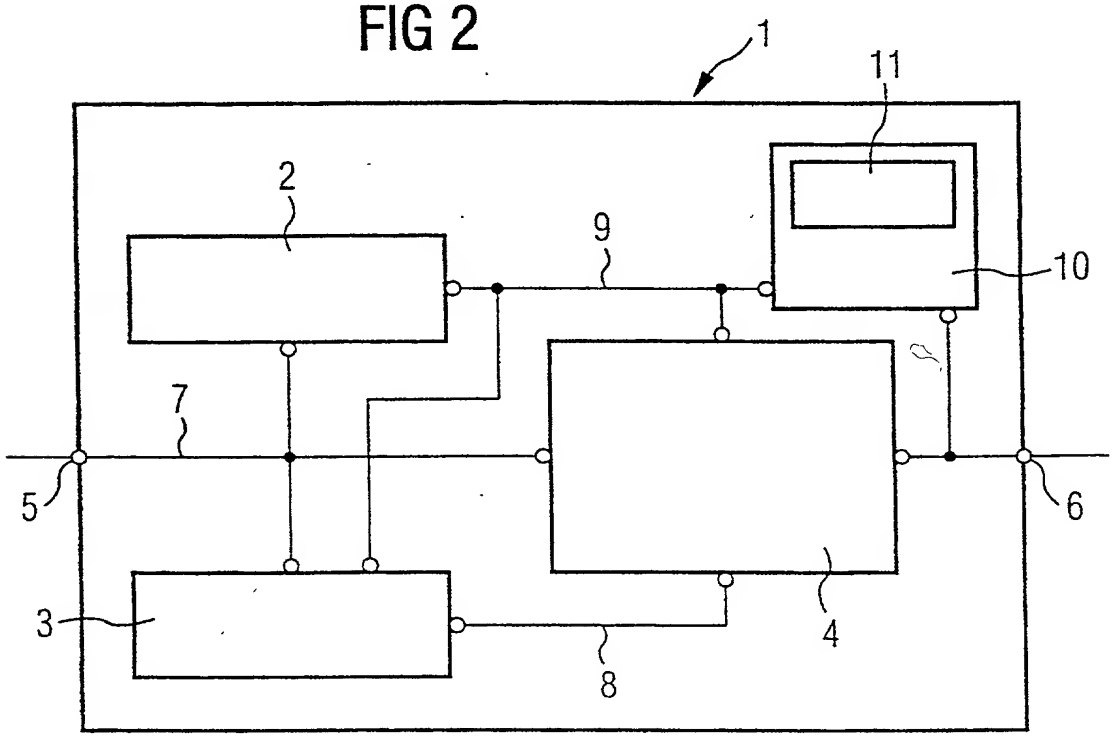


FIG 3

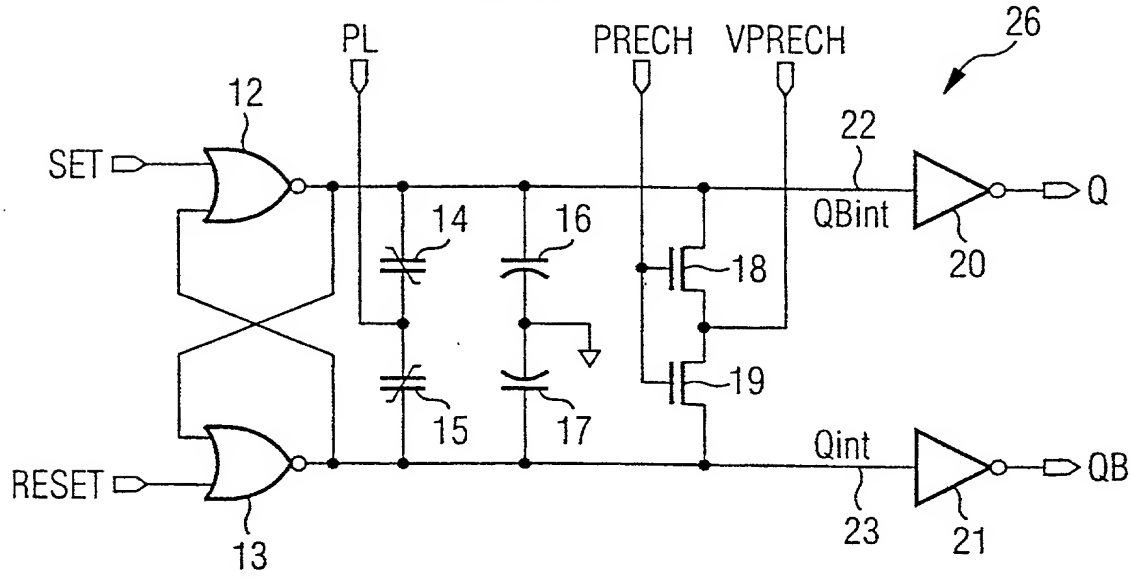

PL
PRECH
VPRECH
26
12
22
SET
Q
14
16
QBint
18
20
19
15
17
Qint
QB
RESET
23
21
13

FIG 4

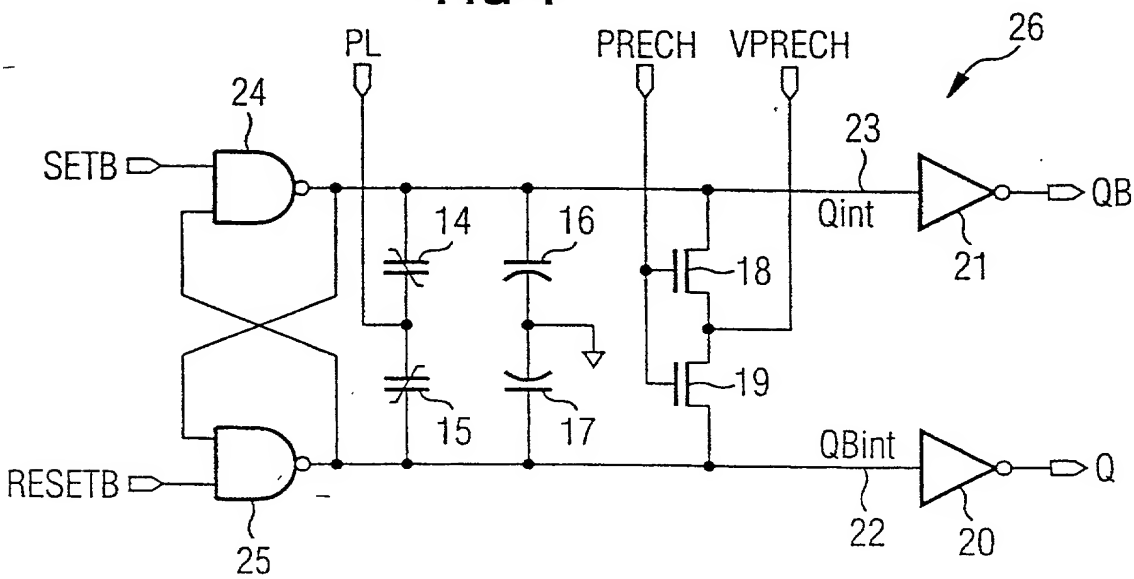
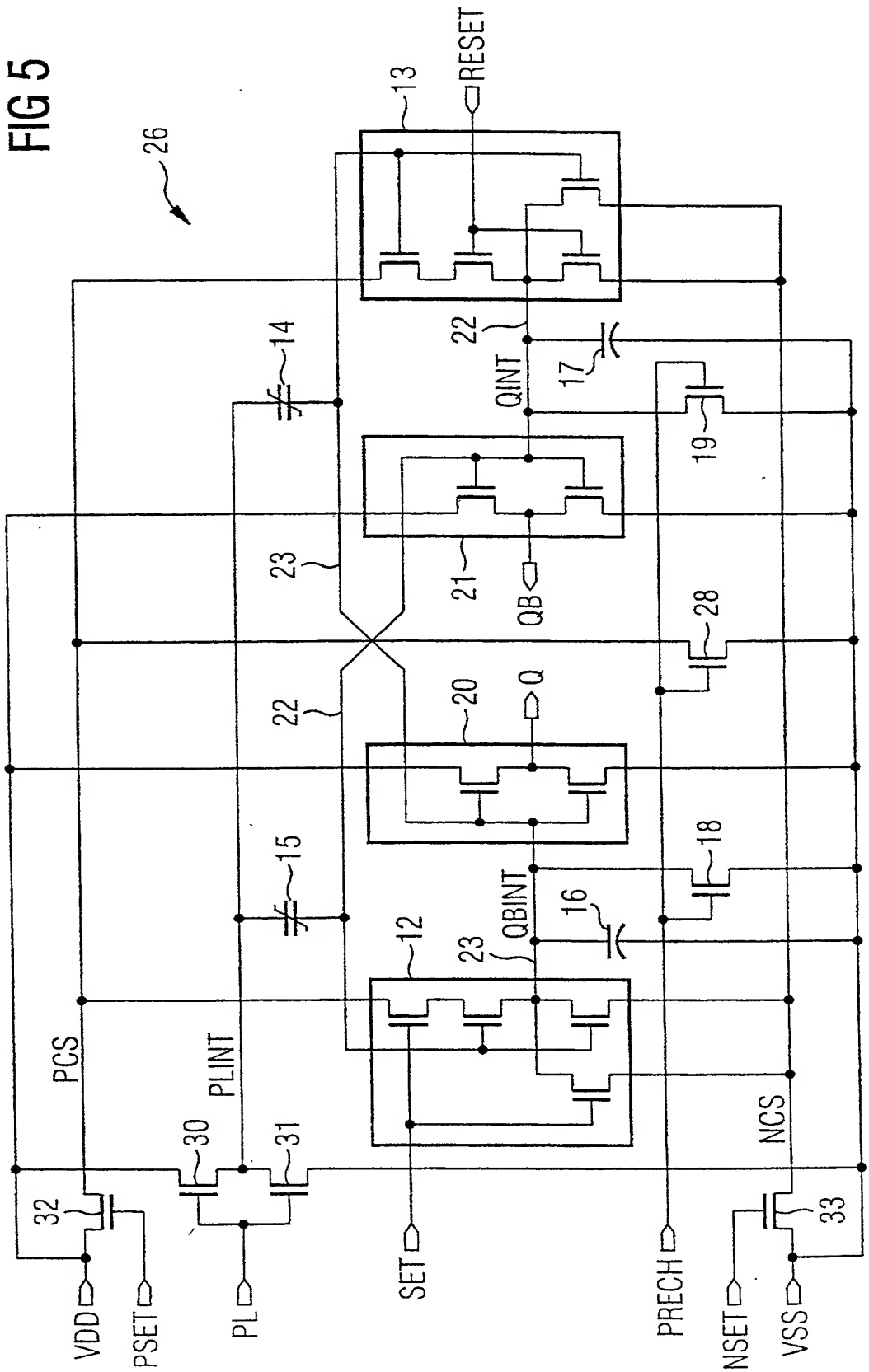

PL
PRECH
VPRECH
26
24
23
SETB
QB
14
16
Qint
18
21
19
15
17
QBint
Q
RESETB
22
20
25

FIG 5


26
13
RESET
14
22
QINT
17
19
23
21
QB
28
22
20
Q
15
18
QBINT
16
12
23
PCS
PLINT
30
31
NCS
32
33
VDD
PSET
PL
SET
PRECH
NSET
VSS

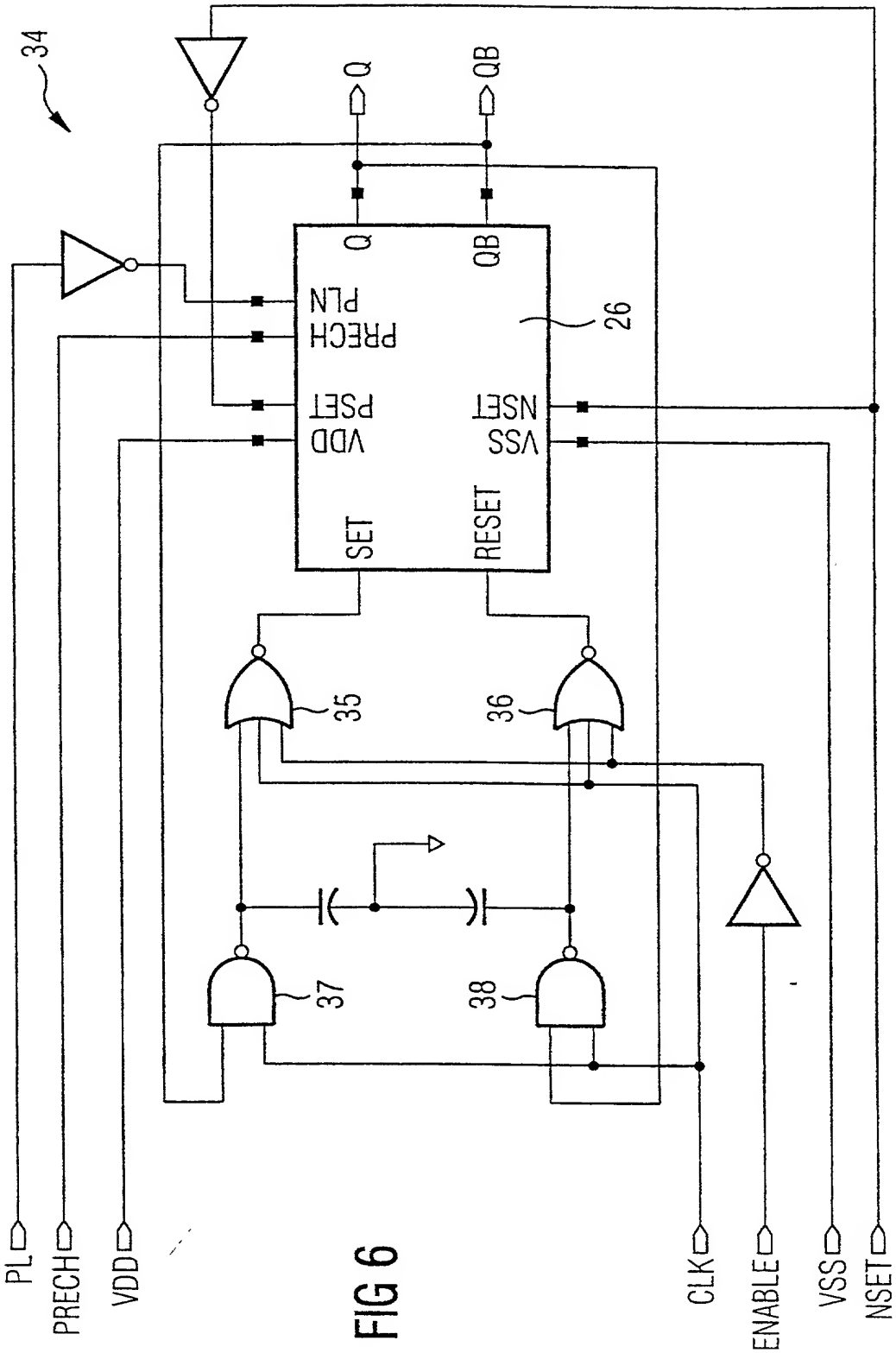

34
Q
QB
Q
QB
PLN
PRECH
PSET
VDD
SET
RESET
NSET
VSS
26
35
36
37
38
PL
PRECH
VDD
CLK
ENABLE
VSS
NSET

FIG 6

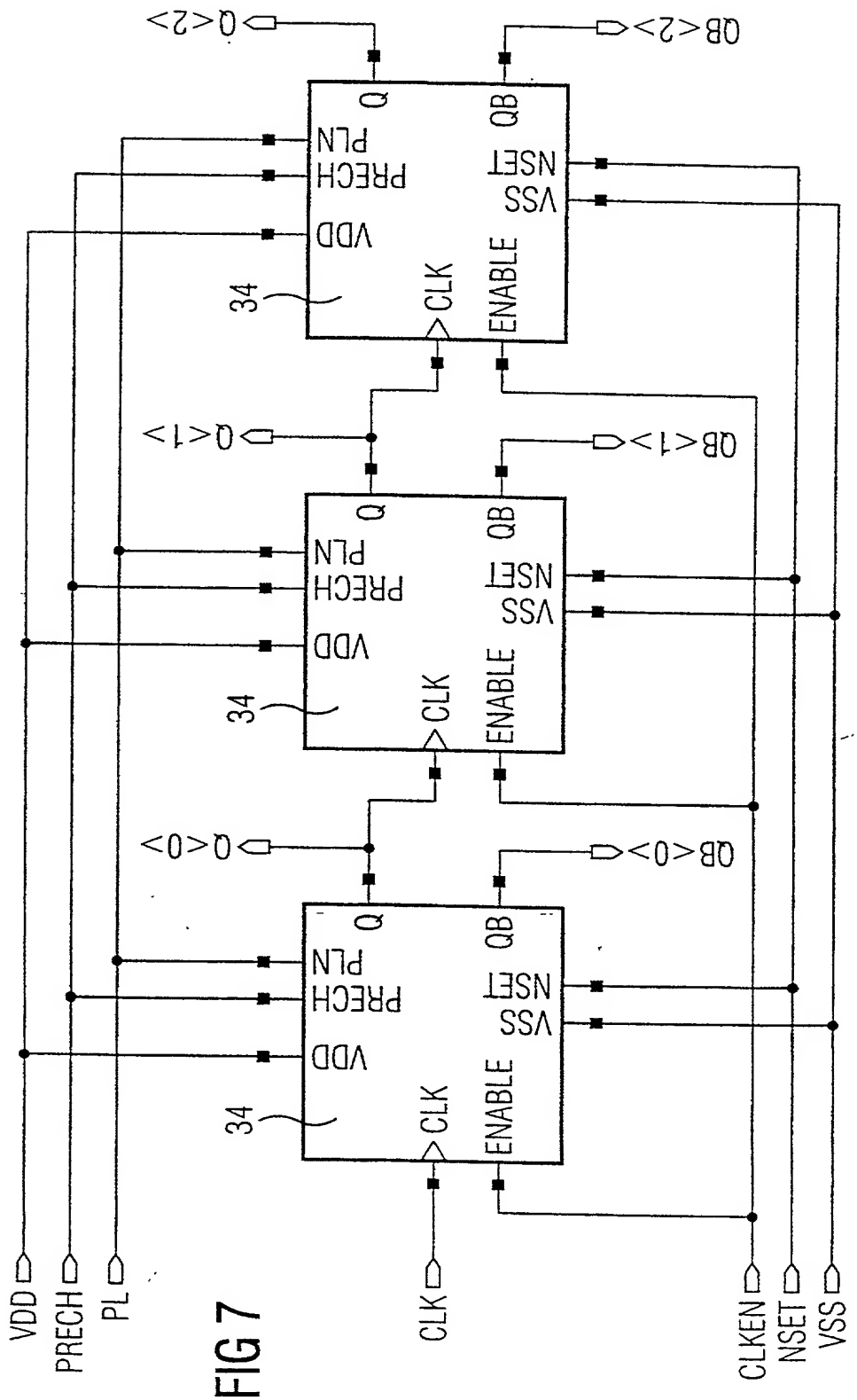

Q<2>
QB<2>
Q
QB
PLN
PRECH
NSET
VSS
VDD
34
CLK
ENABLE
Q<1>
QB<1>
Q<0>
QB<0>
VDD
PRECH
PL
CLK
CLKEN
NSET
VSS

FIG 7

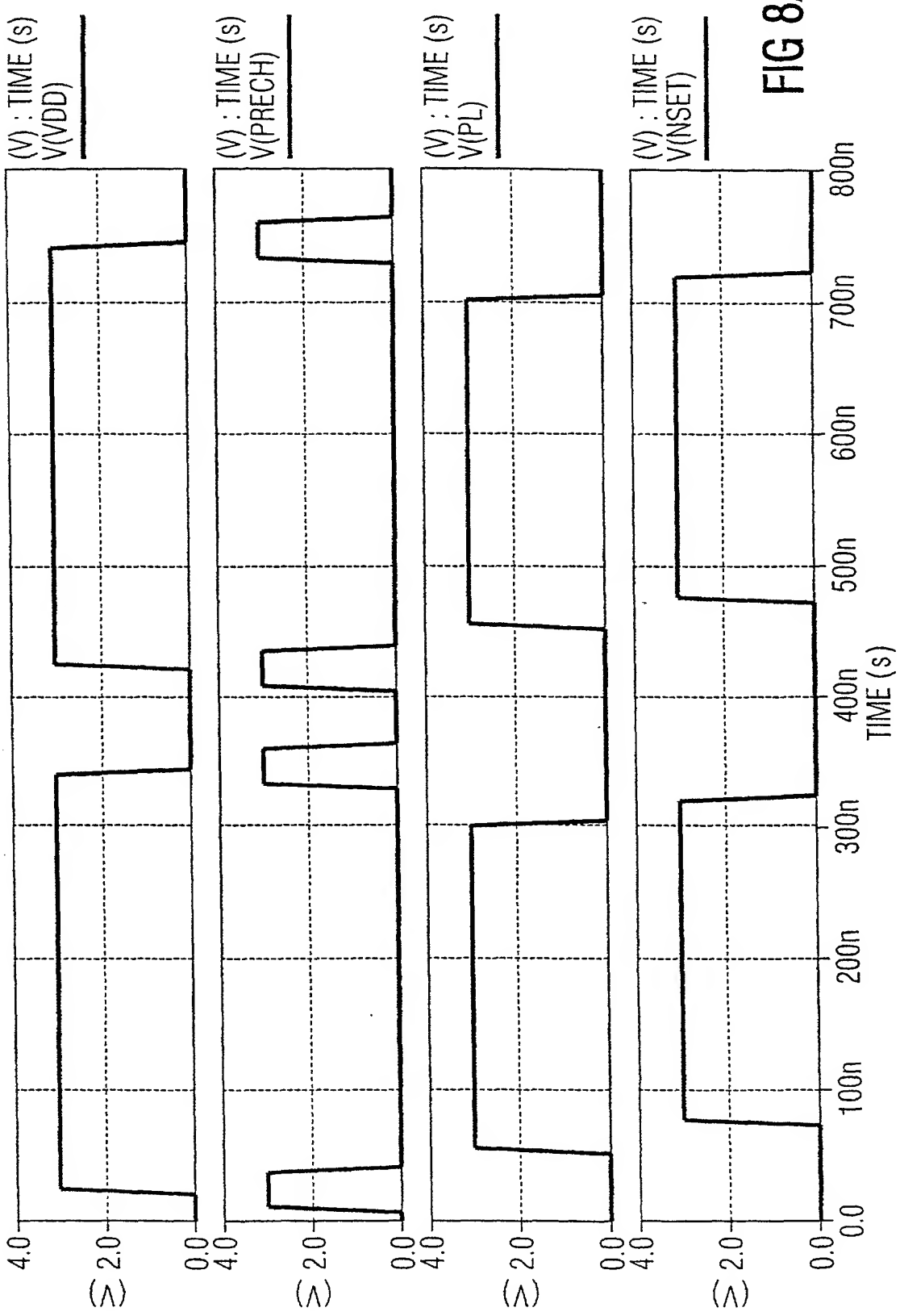

(V) : TIME (s)
V(VDD)
(V) : TIME (s)
V(PRECH)
(V) : TIME (s)
V(PL)
(V) : TIME (s)
V(NSET)
4.0
2.0
0.0
(V)
0.0
100n
200n
300n
400n
500n
600n
700n
800n
TIME (s)

FIG 8A

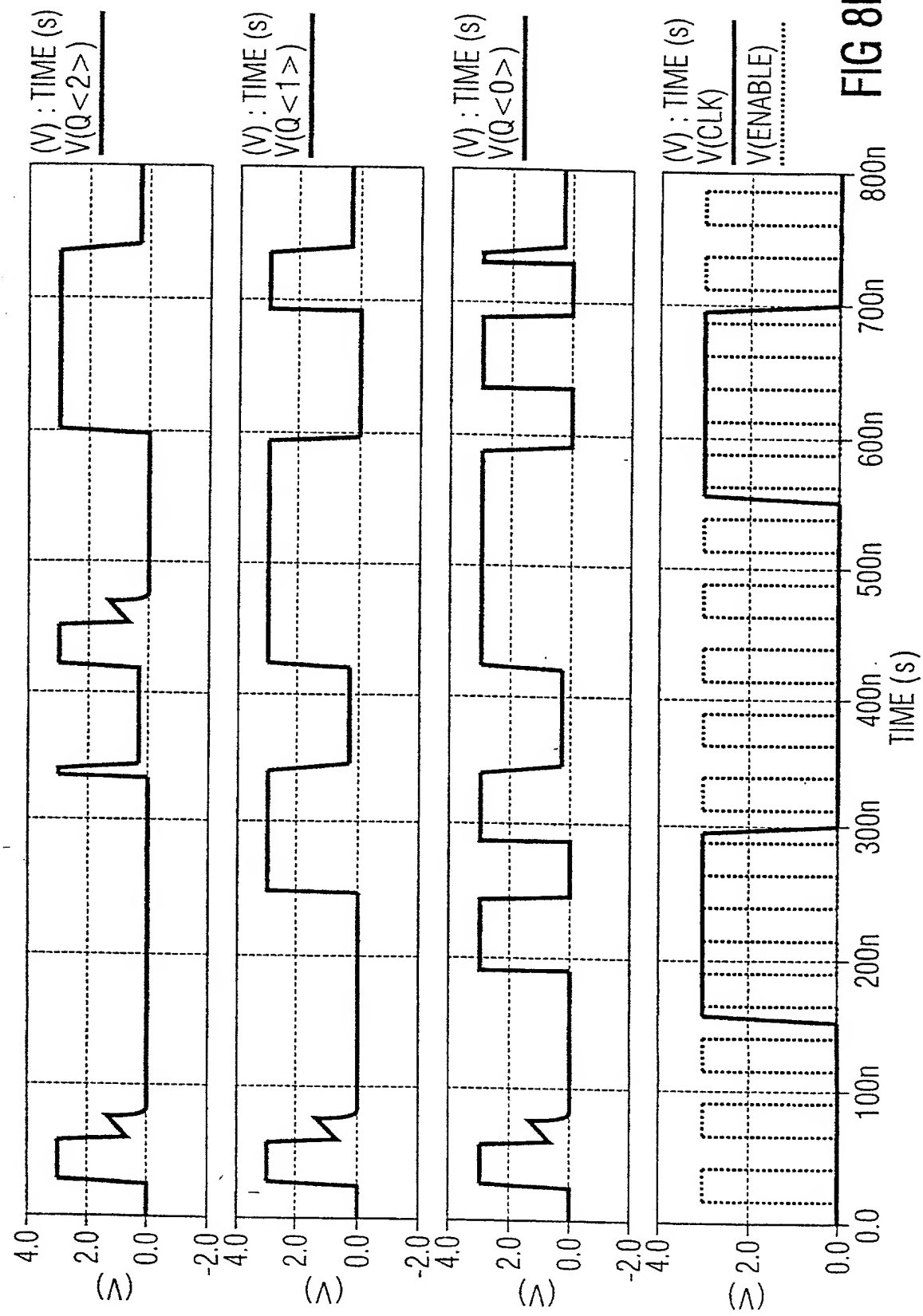

(V) : TIME (s)
V(Q<2>)
(V) : TIME (s)
V(Q<1>)
(V) : TIME (s)
V(Q<0>)
(V) : TIME (s)
V(CLK)
V(ENABLE)
4.0
2.0
0.0
-2.0
(V)
0.0
100n
200n
300n
400n
500n
600n
700n
800n
TIME (s)

FIG 8B

10 Rec'd PCT/PTO 14 MAY 2002

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#5

PTO/SB/103 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Erklärung für Patentanmeldungen mit Vollmacht

German Language Declaration

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My residence, post office address and citizenship are as stated next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Elektronische Schaltung mit ferroelektrischen Flipflops

_____

the specification of which is attached heretounless the following box is checked:

☒ was filed on February 25, 2002
as United States Application Number or PCT
International Application Number 10/070025
_____ and was amended on
_____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

German Language Declaration

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I hereby claim foreign priority under Title 35, 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Applications
(Frühere ausländische Anmeldungen)

Priority Not Claimed
Priorität nicht beanspruct

(Number) (Nummer)	(Country) (Land)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)	☐
19940355.4	Germany	25 August 1999	
_____	_____	_____	☐

Ich beanspruche hiermit Prioritatsvorteile unter Title 35, US-Code, § 119(e) aller US-Hilfsanmeldungen wie unten aufgezählt.

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s)listed below.

(Application No.) (Aktenzeichen)	(Filing Date) (Anmeldetag)
_____	_____
_____	_____

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I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

(Application No.) (Aktenzeichen)	(Filing Date) (Anmeldetag)	(Status) (patented, pending, abandoned) (Status) (patentiert, schwebend, aufgegeben)
PCT/DE00/01607	May 18, 2000	_____
_____	_____	_____

Ich erkläre hiermit, daß alle in der vorliegenden Erklarung von mir gemachten Angaben nach bestem Wissen und Gewissen der Wahrheit entsprechen, und ferner daß ich diese eidesstattliche Erklarung in Kenntnis dessen ablege, daß wissentlich und vorsätzlich falsche Angaben oder dergleichen gemäß § 1001, Title 18 des US-Code strafbar sind und mit Geldstrafe und/oder Gefangnis bestraft werden können und daß derartige wissentlich und vorsätzlich falsche Angaben die Rechtswirksamkeit der vorliegenden Patentanmeldung oder eines aufgrund deren erteilten Patentes gefährden konnen.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

German Language Declaration

VERTRETUNGSVOLMACHT: Als benannter Erfinder beauftrage ich hiermit den (die) nachstehend aufgeführten Patentanwalt (Patentanwälte) und/oder Vertreter mit der Verfolgung der vorliegenden Patentanmeldung sowie mit der Abwicklung aller damit verbundenen Angelegenheiten vor dem US-Patent- und Markenamt: *(Name(n) und Registrationsnummer(n) auflisten)*

Postanschrift:

Telefonische Auskünfte: (*Name und Telefonnummer*)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: (*list name and registration number*)

Gerald E. Helget - #30,948
Nelson R. Capes - #37,106
Kevin W. Cyr - #40,976
Kurt J. Niederluecke - #40,102
Jeffrey R. Stone - #47,976

Send Correspondence to:

Jeffrey R. Stone
BRIGGS AND MORGAN
2200 First National Bank Building
332 Minnesota Street
St. Paul, MN 55101
(651) 223-6600 **(Attorney Docket No. 32226.17)**

Direct Telephone Calls to: (*name and telephone number*)

Jeffrey R. Stone (651) 223-6600

Vor- und Zuname des einzigen oder ersten Erfinders	Full name of sole or first inventor Christl Lauterbach
Unterschrift des Erfinders Datum	Inventor's signature Date 6. May 2002
Wohnsitz	Residence Rosenstr. 6, 85635 Hoehenkirchen-Siegertsbr
Staatsangehörigkeit	Citizenship Germany DE
Postanschrift	Post Office Address
Vor- und Zuname des zweiten Miterfinders (falls zutreffend)	Full name of second joint inventor, if any Georg Braun
Unterschrift des zweiten Erfinder Datum	Second Inventor's signature Date
Wohnsitz	Residence Theresienhoehe 6B, 80339 Munchen
Staatsangehörigkeit	Citizenship Germany
Postanschrift	Post Office Address
Vor- und Zuname des zweiten Miterfinders (falls zutreffend)	Full name of third joint inventor, if any Udo Ollert
Unterschrift des zweiten Erfinder Datum	Third Inventor's signature Date
Wohnsitz	Residence Ahornstr. 1, 84558 Kirchweidach
Staatsangehörigkeit	Citizenship Germany

Postanschrift 4-00	Post Office Address
Vor- und Zuname des zweiten Miterfinders (falls zutreffend)	Full name of fourth joint inventor, if any Werner Weber
Unterschrift des zweiten Erfinder Datum	Fourth Inventor's signature [signature] Date May 3rd, 2002
Wohnsitz	Residence Franz-Marc-Str 6/3, 80637 Munchen DE
Staatsangehörigkeit	Citizenship Germany
Postanschrift	Post Office Address

(Im Falle dritter und weiterer Miterfinder sind die entsprechenden Informationen und Unterschriften hinzuzufügen.)

(Supply similar information and signature for third and subsequent joint inventors.)

1394033v1

10 Rec'd PCT/PTO 14 MAY 2002

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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney for Patent Application
Erklärung für Patentanmeldungen mit Vollmacht

German Language Declaration

Als nacshstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

daß mein Wohnsitz, meine Postanschrift und meine Staatsangehörigkeit den im nachstehenden nach meinem Namen aufgeführten Angaben entsprechen, daß ich nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den den ein Patent für die Erfindung mit folgendem Titel beantragt wird:

_____

_____

deren Beschreibung hier beigefügt ist, es sei denn (in diesem Falle Zutreffendes bitte ankreuzen), diese Erfindung

☐ wurde angemeldet am _____
unter der US-Anmeldenummer oder unter der
Internationalen Anmeldenummer im Rahmen des
Vertrags über die Zusammenarbeit auf dem Gebiet
des Patentwesens (PCT)
_____ und am
_____ abgeändert (falls zutreffend).

Ich bestätige hiermit, daß ich den Inhalt der oben angegebenen Patentanmeldung, einschließlich der Ansprüche, die eventuell durch einen oben erwähnten Zusatzantrag abgeändert wurde, durchgesehen und verstanden habe

Ich erkenne meine Pflicht zur Offenbarung jeglicher Informationen an, die zur Prüfung der Patentfähigkeit in Einklang mit Titel 37, Code of Federal Regulations, § 1.56 von Belang sind.

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Elektronische Schaltung mit ferroelektrischen Flipflops

_____

the specification of which is attached heretounless the following box is checked:

☒ was filed on February 25, 2002
as United States Application Number or PCT
International Application Number 10/070025
_____ and was amended on
_____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

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Date of Deposit 5-14-02
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Mary A. Florin
(Typed or printed name of person mailing paper or fee)
Mary A. Florin
(Signature of person mailing paper or fee)

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German Language Declaration

Ich beanspruche hiermit auslandische Prioritätsvorteile gemäß Title 35, United States Code, § US-Code, § 119 (a)-(d), bzw. § 365(b) aller unten aufgeführten Auslandsanmeldungen für Patente oder Erfinderurkunden, oder § 365(a) aller PCT internationalen Anmeldungen, welche wenigstens ein Land ausser den Vereinigten Staaten von Amerika benennen, und habe nachstehend durch ankreuzen sämtliche Auslands- anmeldungen für Patente bzw. Erfinderurkunden oder PCT internationale Anmeldungen angegeben, deren Anmeldetag dem der Anmeldung, für welche Priorität beansprucht wird, vorangeht.

I hereby claim foreign priority under Title 35, 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Applications
(Frühere ausländische Anmeldungen)

		Priority Not Claimed / Priorität nicht beanspruct
19940355.4 (Number) (Nummer)	Germany (Country) (Land)	
25 August 1999 (Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)		☐
____ (Number) (Nummer)	____ (Country) (Land)	
____ (Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)		☐

Ich beanspruche hiermit Prioritätsvorteile unter Title 35, US-Code, § 119(e) aller US-Hilfsanmeldungen wie unten aufgezählt.

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s)listed below.

____ (Application No.) (Aktenzeichen)	____ (Filing Date) (Anmeldetag)
____ (Application No.) (Aktenzeichen)	____ (Filing Date) (Anmeldetag)

Ich beanspruche hiermit die mir unter Title 35, US-Code, § 120 zustehenden Vorteile aller unten aufgeführten US-Patentanmeldungen bzw. § 365(c) aller PCT internationalen Anmeldungen, welche die Vereinigten Staaten von Amerika benennen, und erkenne, insofern der Gegenstand eines jeden früheren Anspruchs dieser Patentanmeldung nicht in einer US-Patentanmeldung, bzw. PCT internationalen Anmeldung in in einer gemäß dem ersten Absatz von Title 35, US-Code, § 112 vorgeschriebenen Art und Weise offenbart wurde, meine Pflicht zur Offenbarung jeglicher Informationen an, die zur Prüfung der Patentfähigkeit in Einklang mit Title 37, Code of Federal Regulations, § 1.56 von Belang sind und die im Zeitraum zwischen dem Anmeldetag der früheren Patentanmeldung und dem nationalen oder im Rahmen des Vertrags über die Zusammenarbeit auf dem Gebiet des Patentwesen (PCT) gültigen internationalen Anmeldetags bekannt geworden sind.

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

PCT/DE00/01607 (Application No.) (Aktenzeichen)	May 18, 2000 (Filing Date) (Anmeldetag)
____ (Application No.) (Aktenzeichen)	____ (Filing Date) (Anmeldetag)

____ (Status) (patented, pending, abandoned) (Status) (patentiert, schwebend, aufgegeben)	
____ (Status) (patented, pending, abandoned) (Status) (patentiert, schwebend, aufgegeben)	

Ich erkläre hiermit, daß alle in der vorliegenden Erklärung von mir gemachten Angaben nach bestem Wissen und Gewissen der Wahrheit entsprechen, und ferner daß ich diese eidesstattliche Erklärung in Kenntnis dessen ablege, daß wissentlich und vorsätzlich falsche Angaben oder dergleichen gemäß § 1001, Title 18 des US-Code strafbar sind und mit Geldstrafe und/oder Gefängnis bestraft werden können und daß derartige wissentlich und vorsätzlich falsche Angaben die Rechtswirksamkeit der vorliegenden Patentanmeldung oder eines aufgrund deren erteilten Patentes gefährden konnen.

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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Postanschrift:

Telefonische Auskünfte: (*Name und Telefonnummer*)

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St. Paul, MN 55101

(651) 223-6600 **(Attorney Docket No. 32226.17)**

Direct Telephone Calls to: (*name and telephone number*)

Jeffrey R. Stone (651) 223-6600

Vor- und Zuname des einzigen oder ersten Erfinders	Full name of sole or first inventor Christl Lauterbach
Unterschrift des Erfinders Datum	Inventor's signature Date
Wohnsitz	Residence Rosenstr. 6, 85635 Hoehenkirchen-Siegertsbr
Staatsangehörigkeit	Citizenship Germany
Postanschrift	Post Office Address
Vor- und Zuname des zweiten Miterfinders (falls zutreffend) 2-02	Full name of second joint inventor, if any Georg Braun
Unterschrift des zweiten Erfinder Datum	Second Inventor's signature Georg Braun Date April 19th, 2002
Wohnsitz	Residence Theresienhoehe 6B, 80339 Munchen DE
Staatsangehörigkeit	Citizenship Germany
Postanschrift	Post Office Address
Vor- und Zuname des zweiten Miterfinders (falls zutreffend)	Full name of third joint inventor, if any Udo Ollert
Unterschrift des zweiten Erfinder Datum	Third Inventor's signature Date
Wohnsitz	Residence Ahornstr. 1, 84558 Kirchweidach
Staatsangehörigkeit	Citizenship Germany

Postanschrift	Post Office Address
Vor- und Zuname des zweiten Miterfinders (falls zutreffend)	Full name of fourth joint inventor, if any Werner Weber
Unterschrift des zweiten Erfinder Datum	Fourth Inventor's signature Date
Wohnsitz	Residence Franz-Marc-Str 6/3, 80637 Munchen
Staatsangehörigkeit	Citizenship Germany
Postanschrift	Post Office Address

(Im Falle dritter und weiterer Miterfinder sind die entsprechenden Informationen und Unterschriften hinzuzufügen.)

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Erklärung für Patentanmeldungen mit Vollmacht

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Internationalen Anmeldenummer im Rahmen des
Vertrags über die Zusammenarbeit auf dem Gebiet
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_____ und am
_____ abgeändert (falls zutreffend).

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Ich erkenne meine Pflicht zur Offenbarung jeglicher Informationen an, die zur Prüfung der Patentfähigkeit in Einklang mit Titel 37, Code of Federal Regulations, § 1.56 von Belang sind.

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My residence, post office address and citizenship are as stated next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Elektronische Schaltung mit ferroelektrischen Flipflops

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as United States Application Number or PCT
International Application Number 10/070025
_____ and was amended on
_____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

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Date of Deposit 5-14-02
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Mary A. Florin
(Typed or printed name of person mailing paper or fee)

Mary A. Florin
(Signature of person mailing paper or fee)

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German Language Declaration

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Prior Foreign Applications
(Frühere ausländische Anmeldungen)

19940355.4	Germany	25 August 1999	☐
(Number) (Nummer)	(Country) (Land)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)	
____	____	____	☐
(Number) (Nummer)	(Country) (Land)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)	

Ich beanspruche hiermit Prioritätsvorteile unter Title 35, US-Code, § 119(e) aller US-Hilfsanmeldungen wie unten aufgezählt.

____	____
(Application No.) (Aktenzeichen)	(Filing Date) (Anmeldetag)
____	____
(Application No.) (Aktenzeichen)	(Filing Date) (Anmeldetag)

Ich beanspruche hiermit die mir unter Title 35, US-Code, § 120 zustehenden Vorteile aller unten aufgeführten US-Patentanmeldungen bzw. § 365(c) aller PCT internationalen Anmeldungen, welche die Vereinigten Staaten von Amerika benennen, und erkenne, insofern der Gegenstand eines jeden früheren Anspruchs dieser Patentanmeldung nicht in einer US-Patentanmeldung, bzw. PCT internationalen Anmeldung in in einer gemäß dem ersten Absatz von Title 35, US-Code, § 112 vorgeschriebenen Art und Weise offenbart wurde, meine Pflicht zur Offenbarung jeglicher Informationen an, die zur Prüfung der Patentfähigkeit in Einklang mit Title 37, Code of Federal Regulations, § 1.56 von Belang sind und die im Zeitraum zwischen dem Anmeldetag der früheren Patentanmeldung und dem nationalen oder im Rahmen des Vertrags über die Zusammenarbeit auf dem Gebiet des Patentwesen (PCT) gültigen internationalen Anmeldetags bekannt geworden sind.

PCT/DE00/01607	May 18, 2000	____	
(Application No.) (Aktenzeichen)	(Filing Date) (Anmeldetag)	(Status) (patented, pending, abandoned) (Status) (patentiert, schwebend, aufgegeben)	
____	____	____	
(Application No.) (Aktenzeichen)	(Filing Date) (Anmeldetag)	(Status) (patented, pending, abandoned) (Status) (patentiert, schwebend, aufgegeben)	

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Priority Not Claimed
Priorität nicht beanspruct

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s)listed below.

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

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PTO/SB/103 (8-96)
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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

German Language Declaration

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Postanschrift:

Telefonische Auskünfte: (*Name und Telefonnummer*)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: (*list name and registration number)*

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Nelson R. Capes - #37,106
Kevin W. Cyr - #40,976
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Jeffrey R. Stone - #47,976

Send Correspondence to:

Jeffrey R. Stone
BRIGGS AND MORGAN
2200 First National Bank Building
332 Minnesota Street
St. Paul, MN 55101

(651) 223-6600 **(Attorney Docket No. 32226.17)**

Direct Telephone Calls to: (*name and telephone number*)

Jeffrey R. Stone (651) 223-6600

Vor- und Zuname des einzigen oder ersten Erfinders	Full name of sole or first inventor Christl Lauterbach
Unterschrift des Erfinders Datum	Inventor's signature Date
Wohnsitz	Residence Rosenstr. 6, 85635 Hoehenkirchen-Siegertsbr
Staatsangehörigkeit	Citizenship Germany
Postanschrift	Post Office Address
Vor- und Zuname des zweiten Miterfinders (falls zutreffend)	Full name of second joint inventor, if any Georg Braun
Unterschrift des zweiten Erfinder Datum	Second Inventor's signature Date
Wohnsitz	Residence Theresienhoehe 6B, 80339 Munchen
Staatsangehörigkeit	Citizenship Germany
Postanschrift	Post Office Address
Vor- und Zuname des zweiten Miterfinders (falls zutreffend) 3rd	Full name of third joint inventor, if any Udo Ollert
Unterschrift des zweiten Erfinder Datum X	Third Inventor's signature Date 4/22/02 X
Wohnsitz	Residence Ahornstr. 1, 84558 Kirchweidach DE
Staatsangehörigkeit	Citizenship Germany

Postanschrift	Post Office Address
Vor- und Zuname des zweiten Miterfinders (falls zutreffend)	Full name of fourth joint inventor, if any Werner Weber
Unterschrift des zweiten Erfinder Datum	Fourth Inventor's signature Date
Wohnsitz	Residence Franz-Marc-Str 6/3, 80637 Munchen
Staatsangehörigkeit	Citizenship Germany
Postanschrift	Post Office Address

(Im Falle dritter und weiterer Miterfinder sind die entsprechenden Informationen und Unterschriften hinzuzufügen.)

(Supply similar information and signature for third and subsequent joint inventors.)